Master's Thesis

System-level Transient ESD Noise Monitoring using Off-chip and On-chip Circuits

Wooryong Lee

Department of Electrical Engineering

Graduate School of UNIST

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Wooryong Lee

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Approved by

Advisor
Jingook Kim

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This certifies that the thesis of Wooryong Lee is approved.

06. 10. 2020

signature

Advisor: Jingook Kim

signature

Jeehoon Jeong: Thesis Committee Member #1

signature

Gangil Byun: Thesis Committee Member #2

Abstract

Electrostatic discharge (ESD) is defined as a sudden flow of electric charge between the objects with different electrostatic potentials caused by contact and breakdown of air gap or dielectric layer. In electronic systems, ESD is the remarkable critical issue for reliability of compact and complex integrated circuits (IC) and systems and must be deliberated from the initial design process for the safety of users and wasted cost from damaged products. To analyze the effects by the ESD events, the noise voltages inside the products induced by ESD events can be measured. However, the passive measurement method using cables has some limitations. Various on-die ESD detector circuits have previously been proposed to overcome the limits, providing the useful information for ESD noise analysis. But these circuits require lots of time and cost for design and fabrication, so it is hard to apply from the initial design process.

In this thesis, two approaches are proposed for monitoring the system-level transient ESD noise as the further progress of previous researches regarding the detection of system-level transient ESD event. One is the usage of the off-chip ESD detection module including multiple detection circuits with different thresholds for characterizing the range of ESD noises. The proposed detection circuit utilizes the time delay by RC network and can sense the positive ESD events at power line. The sensing characteristics of the detection circuit against ESD event can be represented as a threshold curve. Utilizing the detection threshold curve, the range of ESD noises can be estimated without measurement. For more specific identification of ESD noise range, the detection module with multiple detection circuits are designed and the more exact estimation of noise range becomes possible, depending on which detection circuits sense the ESD event. The threshold curves of detection module are extracted using transmission line pulse (TLP) signals and validated through ESD current injection tests. After then, as an application to real situation, the system-level transient ESD noises in a commercial solid-state drive (SSD) storage system are characterized and analyzed.

The other approach is the capturing the noise waveform itself like digital oscilloscope. Although the previous on-die ESD detector circuits and the proposed approach provide useful information, it is further demanded to obtain the accurate noise waveforms for more complete analysis. So, an on-die oscilloscope circuit including on-chip ESD event detectors is designed and fabricated in a 180-nm CMOS process. The validation of operation is performed, and the measurement results of on-chip ESD detectors are comparable to the results from circuit simulations. However, the ability of waveform capturing is under the designed specification due to several problems in circuit design process.

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Nomenclature

ADC	Analog-to-digital converter
CBE	Charged board event
CDM	Charged device model
CLK	Clock
CP	Charge pump
DAE	Data array enclosure
DFF	D flip-flop
DLL	Delay-locked loop
DUT	Device under test
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
ESD	Electrostatic discharge
FET	Fast electrical transient
FFT	Fast fourier transform
HBM	Human body model
HMM	Human metal model
LDO	Low-dropout
LED	Light emitting diode
LSB	Least significant bit
MQFP	Metric quad flat pack
MSB	Most significant bit
PCB	Printed circuit board
PFD	Phase frequency detector
IC	Integrated Circuit
I/O	Input and output
SPICE	Simulation program with integrated circuit emphasis
SSD	Solid-state drive
TGL	Transmission gate logic
TLP	Transmission line pulse

I. Introduction

1.1 Introduction to Electrostatic Discharge

The electromagnetic compatibility (EMC) and electromagnetic interference (EMI) of electronic systems become more critical issues as integrated circuits (IC) become smaller and denser, and mobile devices such as cell phone and laptop PC are more popularly used. Among several issues in EMC and EMI, electrostatic discharge (ESD) is one of the remarkable events which is defined as a sudden flow of electrostatic charges between the objects with different electrostatic potentials caused by contact and breakdown of air gap or dielectric layer. When two different materials are rubbed and separated, electrostatic charges are generated on the surface of the two materials by triboelectric effect. These charges can be easily generated by the daily activities of human as shown in Fig. 1 [1]-[2]. Since there is very small capacitance about 150 pF between the human body and the nearby ground, the electric potential of human body can be increased up to several kilo-volts or more than 10 kV on dry winter.

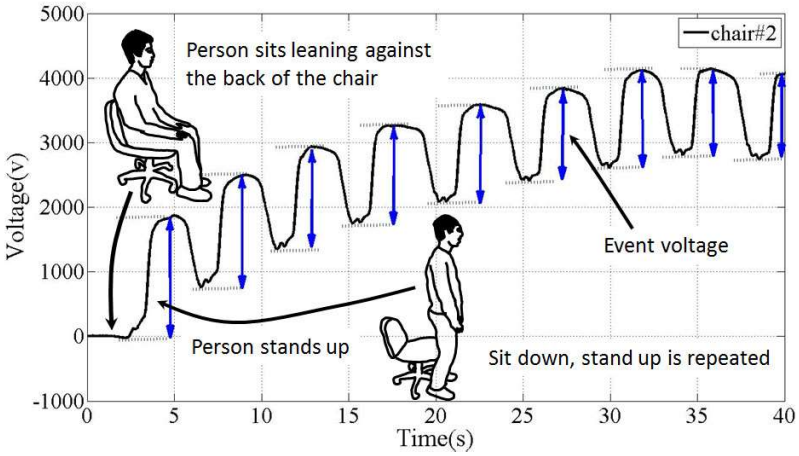


Fig. 1. Electrostatic potential caused by generated charges due to daily activities [1]-[2]

There are several kinds about ESD events according to various circumstances such as human metal model (HMM), human body model (HBM), charged device model (CDM), and charged board event (CBE). As one type of ESD event, Fig. 2 (a) shows a simplified picture of HMM when a charged human injects ESD current to a system through a metal object. As mentioned earlier, the human body can be charged up to several kilo-volts. When the ESD events of HMM occur, the pre-charged high voltages are discharged and high-level current with a fast rise time is injected into the system. Fig. 2 (b) shows the coupled noises in electronic system due to system-level ESD event. These induced ESD noises could cause soft and hard failures of electronic system. Soft failure is impermanent malfunction such as data distortion, latch-up, reboot, and so on. On the other hand, hard failure is defined as permanent damage in the system which cannot be recovered such as breakdown of oxide in semiconductor level. Fig. 3 (a) and (b) depict the examples of soft failure and hard failure from system-level ESD noises, respectively.

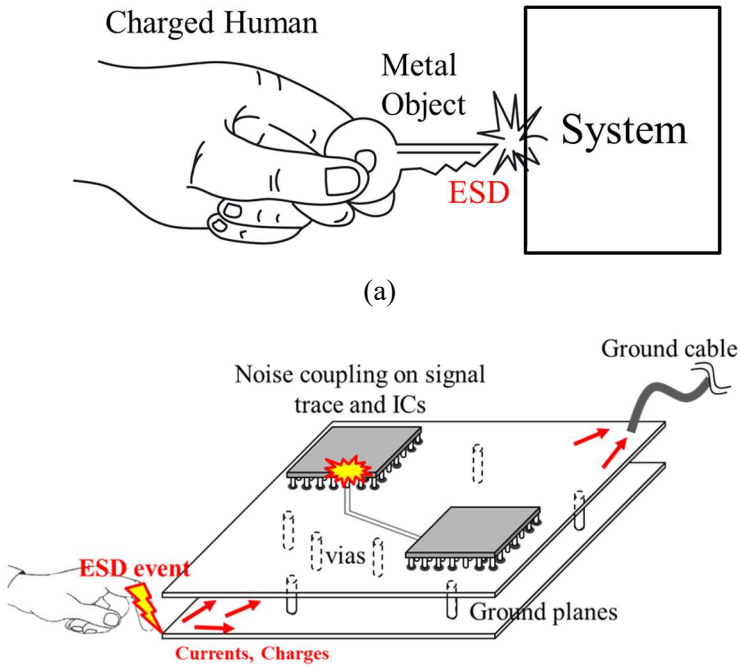


Fig. 2. (a) Simplified picture of human metal model (HMM) (b) The coupled noises due to system-level ESD event

Fig. 3. The examples of (a) soft failure and (b) hard failure from system-level ESD noises

So, the system-level ESD issue should be deliberated from the initial design process for the safety of users and wasted cost from damaged products. There is an international standard for ESD immunity test (IEC 61000-4-2) that every electronic product should pass before launching [3]. Fig. 4 shows an ESD current waveform at 2 kV level according to IEC 61000-4-2. The ESD generator in Fig. 5 is widely used as an ESD test equipment which consists of the ESD gun body and ground strap [4]. The generator imitates ESD events by contact and air discharge. In the contact mode in ESD generator, the generator is pre-charged to several kV and then, if triggered, the charged voltage is collapsed within 1 ns and ESD current flows into the contact point through the internal relay. Fig. 6 (a) shows an example of ESD

immunity test setup for electronic product. In this setup, the ESD current like Fig. 6 (b) is injected according to [3].

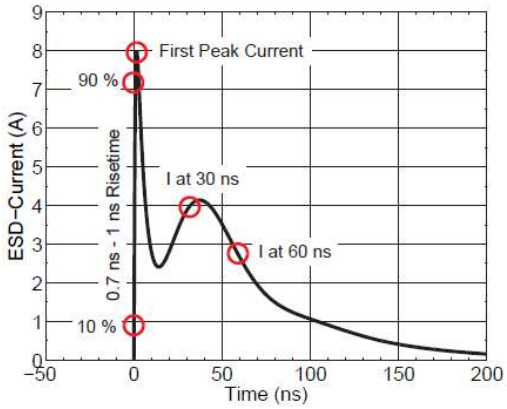
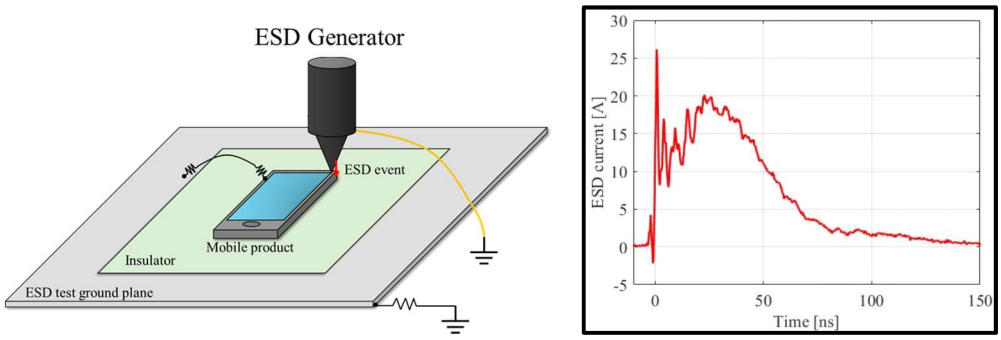


Fig. 4. ESD current waveform at 2 kV level according to IEC 61000-4-2 [3]

(a) (b)

Fig. 5. ESD generator, DITO from EM test, which consists of (a) gun body and (b) ground strap [4]



(a) (b)

Fig. 6. (a) ESD immunity test setup for electronic product (b) The injected ESD current by ESD generator

1.2 Previous Researches

During the ESD immunity test using ESD generator, the ESD-induced noise voltages inside the product can be measured to analyze the effects of the ESD event. In [5], Soft failures in mobile devices due to ESD noises were investigated. The RC low-pass filters were designed and implemented to

improve the ESD immunity and the improved mobile phone's immunity to ESD was verified in measurement. The influence of ESD noises on the electromagnetic susceptibility (EMS) of the IC was analyzed in [6]. In [7], system-level ESD noises and failures of wearable devices were modeled and investigated. The soft failure threshold of a wearable device was compared for two positions, measuring the discharging currents. In [8], statistical operation errors of IC with a D-type flip-flop due to a system-level ESD were analyzed in measurement and SPICE circuit simulations. The effects of decoupling capacitors on the IC operation failures due to ESD were investigated. In [9], system-level ESD noises are measured on a motherboard including IC with delay-locked loop (DLL) and the results are correlated to the jitters of clock signals from DLL.

However, the passive measurement method shown in Fig. 7 has some limitations. At first, installing and soldering the measurement cables could be impossible in complex and compact products. And, the common-mode noises caused by strong electric field under the ESD event should be removed to measure the exact differential-mode voltages. In Fig. 7, several ferrite beads are combined into measurement cables. However, the removal of the common mode noise is incomplete in most cases. Also, the coupled ESD noises to various structures such as wire bonding or IC package are difficult to be included in printed circuit board (PCB)-level measurement.

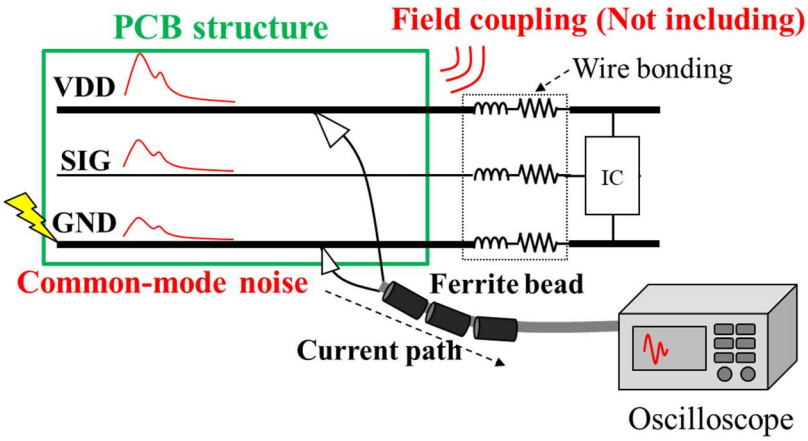


Fig. 7. The passive ESD-induced noise measurement method using cable

A number of previous studies have previously been proposed to avoid the mentioned limits. In [10], the levels of ESD event are detected with combination of a fuse and diode. The occurrence of a electrical stress beyond a set threshold can be sensed by the melt fuse. The noises at power supply created by a transient event are used for detection of the event in [11]-[14]. In [13], the voltage fluctuations at the on-die power supply line is capacitively coupled and the detector senses the ESD event using coupling capacitors and logic latch. A RC-based circuit in [14] also senses the fast electrical transient (FET) at power supply voltage.

In addition to power supply line, the circuits for ESD events at an input and output (I/O) pins have

been proposed using the combination of on-die ESD protection diode and capacitor to store the peak level of an event [15]. In [16] and [17], the sensors are implemented in the I/O pins of a microcontroller. These sensors can be utilized to find when an I/O pin perceives a transient stress event and determine the peak level of noise by the event. In [18], it can be found that these sensors work properly from the experiments in system-level tests. But, the system has to include a microcontroller which has the sensors implemented in its I/O pins for usage. Table 1 summarizes and compares the previous researches with this thesis.

Table 1. Previous Researches

Title	Transient-to-Digital Converter for System-Level Electrostatic Discharge Protection in CMOS ICs	An On-Chip Detector of Transient Stress Events	Measurement and Analysis of System-Level ESD-Induced Jitter in a Delay-Locked Loop	**This work**
Authors	Ming-Dou Ker	Abhishek Patnaik	Myeongjo Jeong	**Wooryong Lee**
Publish (year)	IEEE Transactions on Electromagnetic Compatibility (2009)	IEEE Transactions on Electromagnetic Compatibility (2018)	IEEE Transactions on Electromagnetic Compatibility (2019)	**A master's thesis (2020)**
Main Contribution	ESD event sensing in power supply voltage using *RC*-based circuit	Detection of the transient stress events at I/O pads with ESD protection structures	Measurement of ESD noises on a motherboard for correlating the jitters of DLL clock signals	**Characterization of the ESD noise range and circuit design for noise waveform capturing**

1.3 Objectives of This Thesis

In this thesis, two approaches are proposed for monitoring the system-level transient ESD noise as the further progress of previous researches regarding the detection of system-level transient ESD event. As mentioned, various on-die ESD detector circuits have been proposed to overcome the limits of the passive measurement for ESD noise analysis in complex and compact products. These on-die detector circuits can provide useful but only limited information for analysis such as peak voltage or current levels. Also, these circuits require lots of time and cost for design and fabrication, therefore it is hard to apply from the initial design process.

In section II, the off-chip ESD event detection circuit is proposed for characterizing the range of ESD noise without measurements. The detection circuit utilizes the time delay by RC network like [14] and

can sense the positive ESD events at power line. The characteristics in sensing the ESD event of the detection circuit can be represented as a threshold curve which shows typically the inversely proportional relation between peak level and pulse width of noise pulse. Once the threshold curve of detector circuit is obtained, the range of ESD noises can be estimated without measurement. For better characterization, a detection module including the multiple detection circuits with different detection properties is employed and the more exact estimation of noise range becomes possible, depending on which detection circuits sense the ESD event. The detection threshold curves of detection module are extracted using transmission line pulse (TLP) signals and validated through ESD current injection tests. As an application to real situation, the system-level transient ESD noises in a commercial solid-state drive (SSD) storage system are characterized and analyzed.

In section III, the other approach is proposed for capturing the noise waveform itself like digital oscilloscope. The proposed approach can characterize the noise range, but it still has some problems in size and accuracy. Also, although the on-die circuits from previous researches can provide useful information such as peak voltage or current level or when a transient stress event ocuurs, it is better to know the accurate noise waveforms for the more complete analysis. So, an on-die oscilloscope circuit including on-chip ESD detectors is designed and fabricated in a 180 nm CMOS process. The validation of operation is performed, and the measurement results are compared with the results from circuit simulations.

II. Characterization of ESD Noise Range using Off-chip Detection Module

2.1 Introduction to Off-chip Detection Circuit

The on-die ESD detector circuits from previous researches can provide useful information for analysis of system-level ESD noises such as peak level or occurrence time of ESD events. Also, the detection circuits like [16] and [17] can be utilized with ESD protection structures at I/O pins. Additionally, the detector circuits can be designed and fabricated together with target ICs in system so the accuracy problem at PCB-level measurements does not need to consider. However, these on-die ESD detector circuits require lots of time and cost for design and fabrication. Also, the modification of the circuit is almost impossible because the circuit itself is fixed in fabrication. Therefore, in this section, as an alternative, the off-chip ESD event detection circuit is proposed for characterizing the range of ESD noise without measurement.

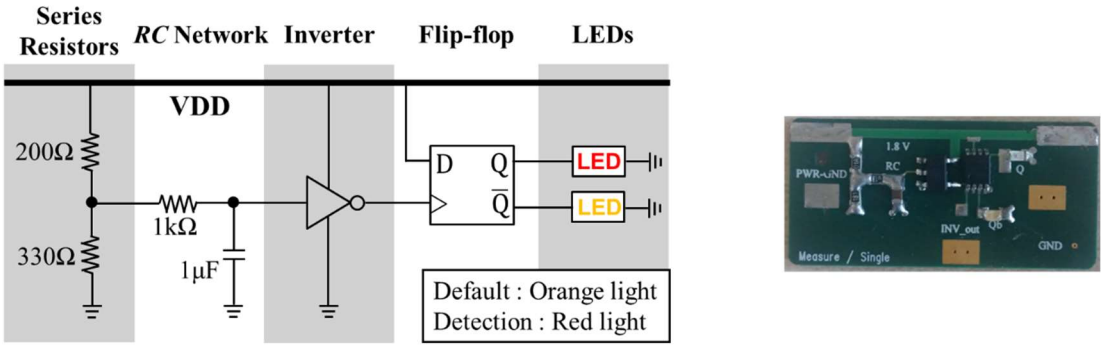


Fig. 8. (a) Schematic of the proposed off-chip detection circuit (b) Implemented circuit on PCB

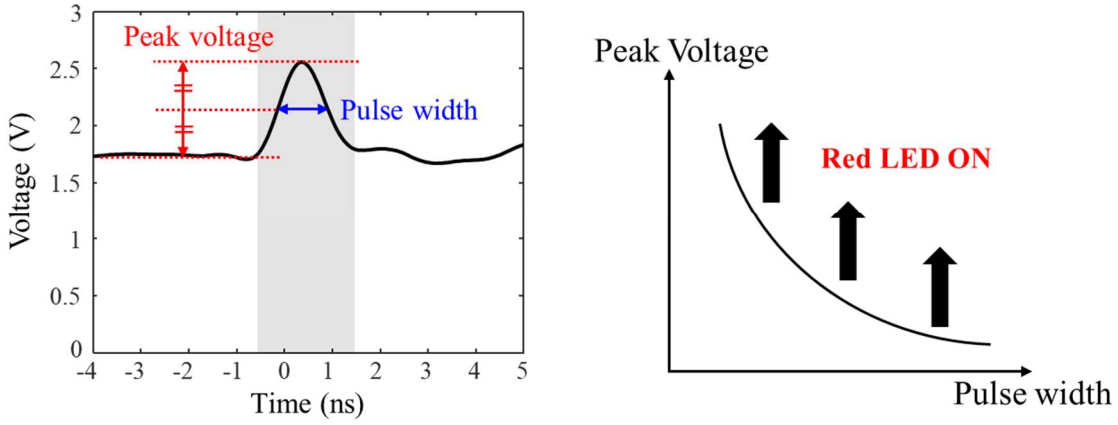
Fig. 8 (a) shows the schematic of the proposed off-chip detection circuit which consists of series resistors, RC network, inverter, D flip-flop (DFF), and light emitting diodes (LED). Similar to [14], this detection circuit is connected in parallel to power supply line of electronic system for detection of the positive ESD events, utilizing the time-delay of RC network. In typical electronic system, ESD noises at power supply line show the ringing shape due to low power distribution network (PDN) impedance. That is, the positive and negative ESD events occur alternately, so the proposed detection circuit doesn't lose the generality in ESD event detection. Fig. 8 (b) is an implemented circuit on PCB where the size of PCB is 25 mm × 12 mm. In normal condition, the levels of V_{REF} and V_A are set as high level to the input of inverter from the series resistors. The output of inverter is low state, and the orange LED is turned-on. When the positive ESD event occurs at VDD, the voltage level at VDD increases rapidly but the level at V_A shows the slower voltage response due to time delay from RC network. Then, the level at V_A is recognized as the relatively low inverter input and the output of inverter is changed from low

to high level. This change positively triggers the flip-flop and the state of Q becomes high state, turning on the red LED. Therefore, the positive ESD event can be sensed from the color of turned-on LED.

2.2 Detection Threshold Curve of Detection Circuit

2.2.1 Extraction of threshold curve using transmission line pulse (TLP)

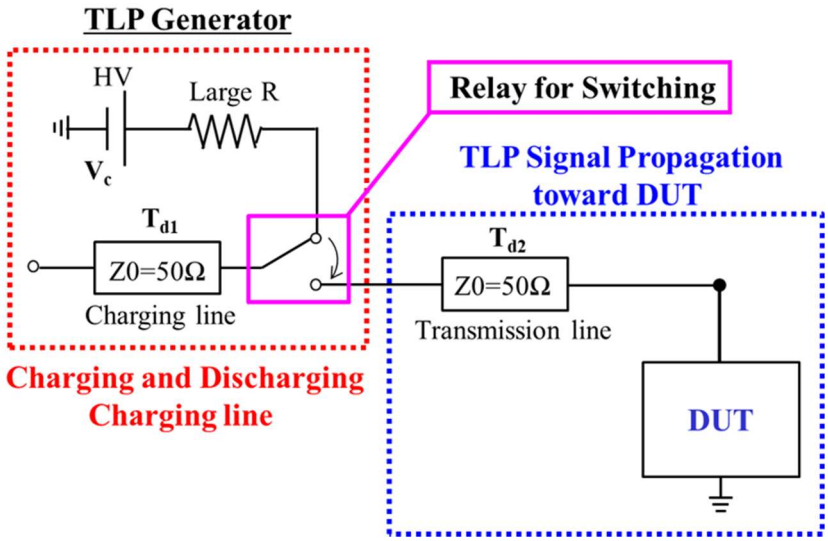
In the proposed detection circuit, the ESD events will be detected only when the strong noise signal is applied to VDD-GND of circuit because the levels of V_{REF} and V_A are set as high level to the input of inverter in normal condition. The detection characteristics of circuit can be represented as a threshold curve for the noise pulses like Fig. 9 (a) where the threshold curve typically shows the inversely proportional relation between peak level and pulse width of noise pulse as shown in Fig. 9 (b). Here, the pulse width is defined as the time duration between two half peaks. When the various noise pulses like Fig. 9 (a) are applied to VDD-GND of circuit, if the peak level and pulse width of noise pulses are confirmed and the color of turned-on LED is checked at each time, the threshold curve can be extracted. After then, according to the turned-on LED color, the range of noise can be identified. For example, if the red LED is turned-on, it means that the noise pulse over threshold curve occurred at VDD-GND.



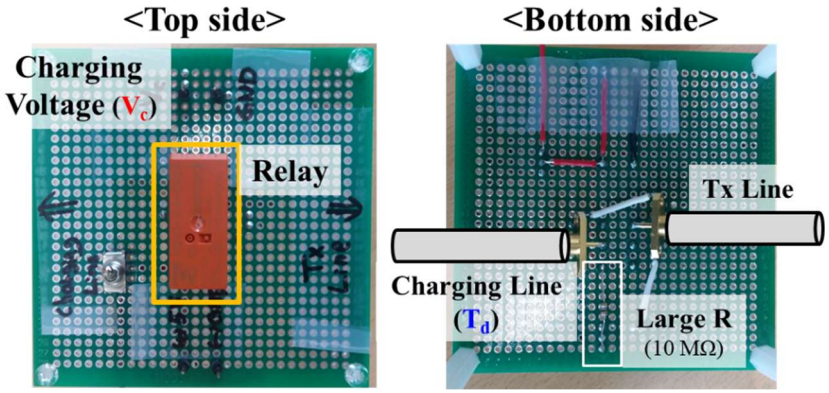
(a) (b)

Fig. 9. (a) Example of a noise pulse (b) The expected threshold curve of detection circuit

To extract threshold curve of detection circuit, the amplitude and pulse width of applied noise pulse need to be controllable. In this thesis, transmission line pulse (TLP) signals are used as noise pulses. Fig. 10 (a) shows the illustration of test setup using TLP generator. The TLP generator operates in two phases according to the switching of relay. In charging phase, the high voltage supply is connected to charging line through large resistance and the charging line is charged. In discharging phase, the charging line and transmission line are connected and TLP signal is propagated toward device under test (DUT). Fig. 10 (b) shows the TLP generator implemented on PCB.



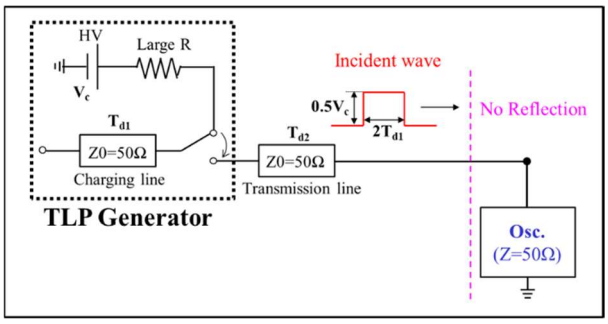
(a)



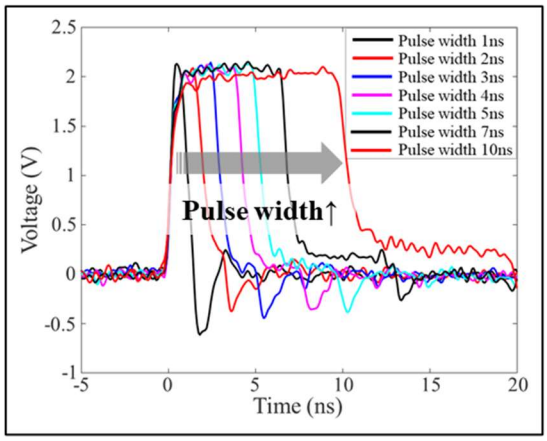
(b)

Fig. 10. (a) Illustration of test setup using TLP generator (b) TLP generator implemented on PCB

The amplitude and pulse width of generated signal in the TLP generator can be adjusted by changing the charging voltage from high voltage supply and the type and length of charging line. In an ideal case, the amplitude of signal is a half of charging voltage and the pulse width is the twice of propagation delay in charging line. Fig. 11 (a) shows the measurement setup for TLP signals with various charging lines. The measured TLP signals with pulse widths from 1ns to 10ns are shown in Fig. 11 (b). Table 2 summarizes the type and length of the used charging lines in this thesis.



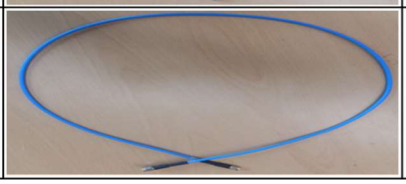
(a)

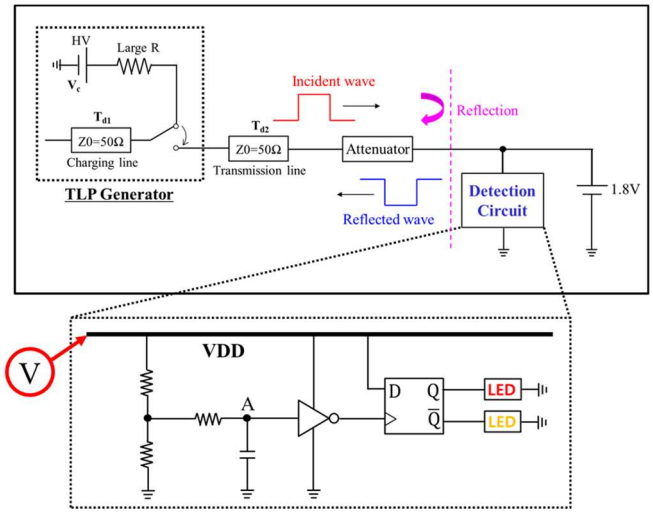


(b)

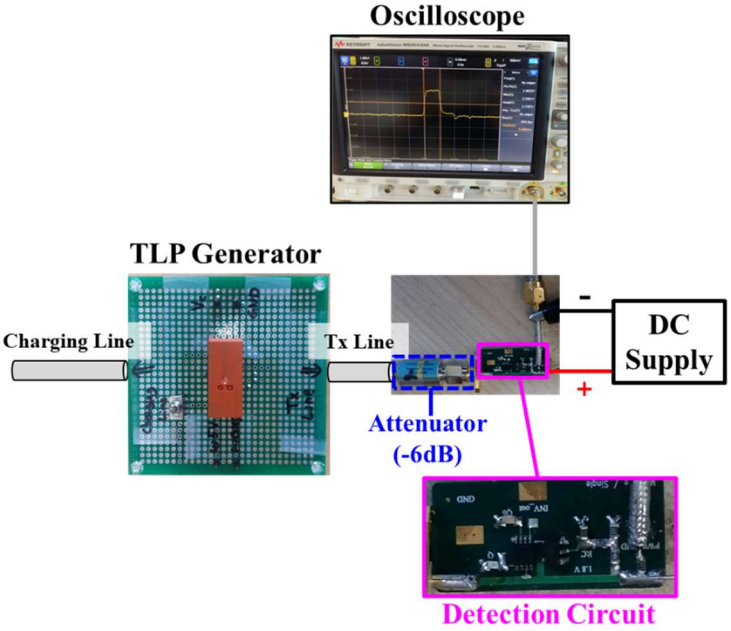
Fig. 11. (a) Measurement setup for TLP signals (b) Measured TLP signals with pulse widths from 1 ns to 10 ns

Table 2. Various type and length of charging lines

Pulse width	Charging Line	Cable Type & Length
1ns		Semi-Rigid Cable 5cm
2ns		RG316 Cable 15cm
3ns		RG316 Cable 15cm +Semi-Rigid Cable 9.5cm
4ns		Semi-Rigid Cable 30cm +Semi-Rigid Cable 8cm
5ns		RG316 Cable 50cm
7ns		RG316 Cable 50cm +RG316 Cable 15cm
10ns		RG402 Cable 1m



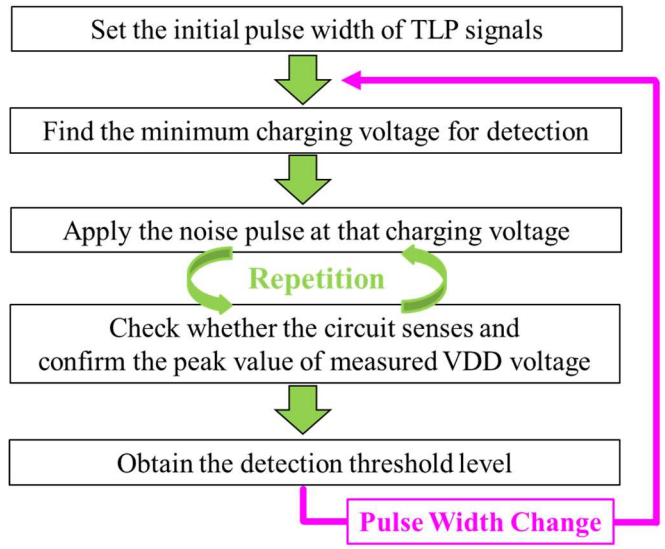
(a)



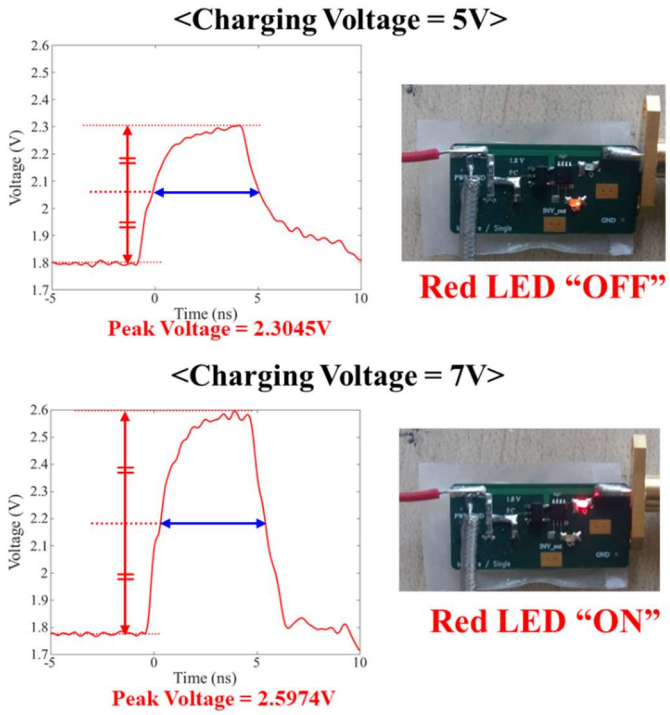
(b)

Fig. 12. Test setup using TLP generator for extracting threshold curve of detection circuit (a) Block diagram (b) Simplified drawing with pictures

Fig. 12 shows the test setup using TLP generator for extracting threshold curve of detection circuit. The TLP signals generated from TLP generator are applied to VDD of detection circuit. Since the impedance is not matched at VDD of circuit, to reduce the effects by reflection, the attenuator is inserted between TLP generator and detection circuit. If the reflection occurs, the reflected signal goes to open-end in TLP generator. At this point, total reflection occurs and this reflected signal with opposite polarity is applied to detection circuit again. But, these reflected signals are attenuated several times passing through the attenuator so the secondly applied signal could be ignorable. In order to confirm the applied noise pulse, the voltage at VDD is measured using the oscilloscope.



(a)



(b)

Fig. 13. (a) Flow chart describing the procedure of threshold curve extraction (b) Two noise pulses with pictures of detection circuit

Fig. 13 (a) is a flow chart describing the procedure of threshold curve extraction. At first, the initial pulse width of TLP signal is decided. As an example, the pulse width is set as 5 ns. It means that the cable corresponding to 5 ns is used as the charging line in TLP generator. And, the minimum charging voltage for detection is found. Starting from the low level, the charging voltage becomes larger and the stronger signals are applied to detection circuit. At certain level of charging voltage, the amplitude of

noise pulse is over threshold and the red LED is turned-on. In Fig. 13(b), when the charging voltage is 5V, the noise pulse is not strong enough to be detected. But, when the charging voltage increases up to 7V, the amplitude of noise pulse is enough for detection, so the red LED is turned-on. Then, the charging voltage is fixed as 7V and the noise pulses are repeatedly applied. At each noise pulse, the LED color is checked and the peak value of measured VDD voltage is confirmed. After the enough repetition, the detection boundary level at 5 ns can be obtained. The procedure up to now is repeated in other pulse width cases. By doing so, the boundary level at each pulse width is obtained and the threshold curve can be drwan.

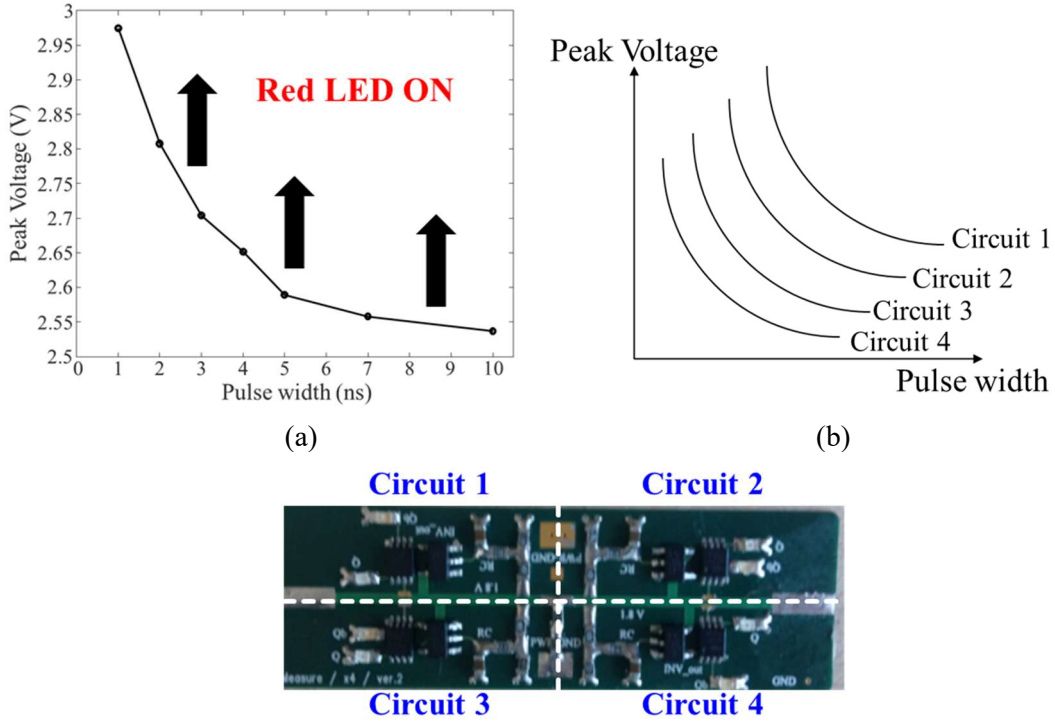
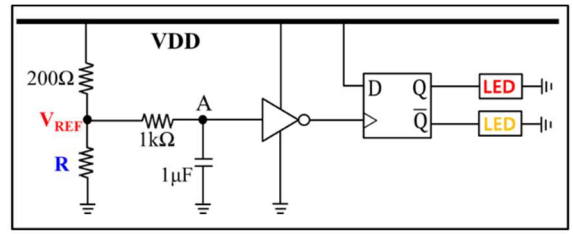


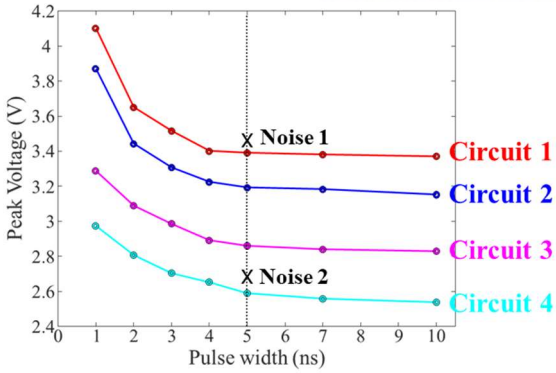
Fig. 14. (a) Characterized detection threshold curve from 1 ns to 10 ns (b) Threshold curves of 4 different detection circuits (c) The designed PCB of detection module including 4 detection circuits

Fig. 14 (a) shows characterized detection threshold curve from 1 ns to 10 ns. For now, by utilizing this threshold curve, the noise range can be estimated by LED color. But the estimated noise range is somewhat broad. For the more specific identification of noise range, the multiple detection circuits can be utilized. If these circuit have different threshold curves like Fig. 14 (b), the range of noise can be identified depending on which circuits sense the noise from the threshold curves. So, the detection module as shown in Fig. 14 (c) is designed where 4 detection circuits, Circuit 1 to Circuit 4, are connected in parallel to common VDD power net. Here, the PCB size is 45 mm × 15 mm.

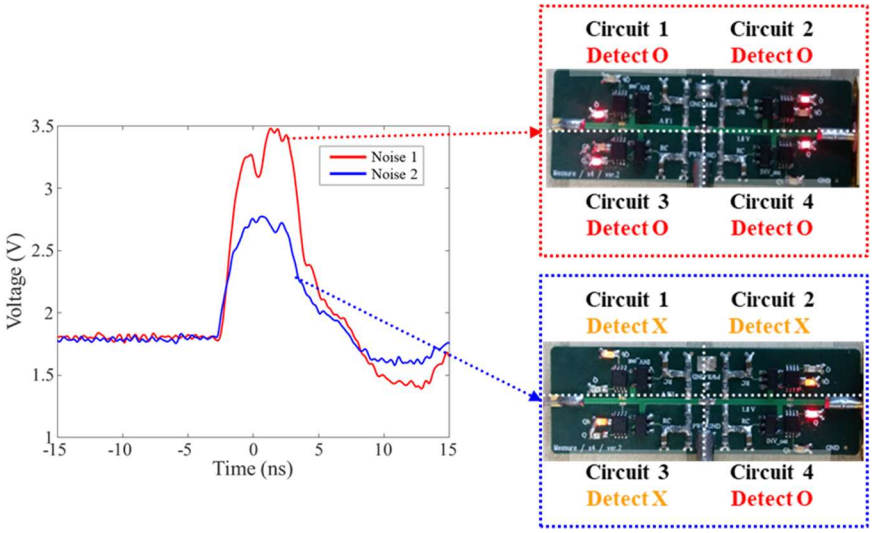


	Circuit 1	Circuit 2	Circuit 3	Circuit 4
R	1.3 kΩ	820 Ω	470 Ω	330 Ω

(a)



(b)



(c)

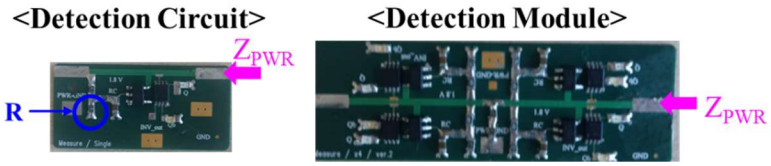
	Circuit 1	Circuit 2	Circuit 3	Circuit 4
R	1.3 kΩ	820 Ω	470 Ω	330 Ω
Noise 1	Detect O	Detect O	Detect O	Detect O
Noise 2	Detect X	Detect X	Detect X	Detect O

(d)

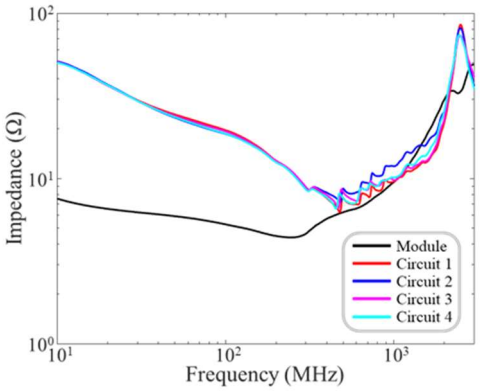
Fig. 15. (a) 4 detection circuits with different resistor values (b) The extracted threshold curves of detection module (c) 2 noise pulses with 5 ns pulse width but different amplitudes and the pictures of module for 2 noise pulses (d) Detection of module for 2 noise pulses

With only changing the value of resistor, 4 detection circuits are decided as shown in Fig. 15 (a). Like a single detection circuit, the procedure for extracting threshold curve is equally applied to detection module. Fig. 15 (b) shows the extracted threshold curves of detection module where Circuit 1 has the highest detection threshold level. Because V_{REF} level of Circuit 1 is higher than that of other circuits in normal condition, the stronger noise is needed for detection. The different point with respect to single detection circuit is that multiple detection circuits in module can detect depending on the noise pulses.

For example, for Noise 1 case in Fig. 15 (c), all circuits can detect this noise pulse because the amplitude is over the threshold level of Circuit 1 as shown in Fig. 16 (b). Fig. 16 (d) is a table representing the detection of module for 2 noise pulses.



(a)



	Circuit 1	Circuit 2	Circuit 3	Circuit 4
R	1.3 kΩ	820 Ω	470 Ω	330 Ω

(b)

Fig. 16. (a) Measurement points for power net impedance (Z_{PWR}) (b) Z_{PWR} of detection circuits and module

Fig. 16 (a) represents measurement points for power net impedance (Z_{PWR}) in detection circuit and module. From vector network analyzer (VNA), S-parameters are measured and converted to Z-parameters. Fig. 16 (b) is Z_{PWR} plots of each detection circuit and module. Z_{PWR} of detection circuits and module are much larger than PDN impedance of typical electronic system which is almost less than 1 Ω. Thus, the detection module can be installed in parallel with a real system with negligible effects. As the next step, the threshold curves from TLP signals are validated using ESD gun.

2.2.2 Validation of threshold curves in ESD current injection tests

In the previous sub-section, the threshold curves of detection module are extracted using TLP signals. Before applying these threshold curves to analysis of system-level ESD noises, the noise source is changed to ESD generator and the validation process is performed. Fig. 17 represents the test setup for validation of threshold curves using ESD gun. In this setup, the power and ground of detection module are connected to those of test PCB where the regulator is installed for supplying the power at VDD of module in Fig. 17 (a). The ESD currents from ESD gun are injected to PCB GND and the ESD noises at common VDD power net of module are measured as shown in Fig. 17 (b). The PCB GND is shorted

to ground plane via copper tape. To prevent the directly coupled ESD noise from ESD gun, the detection module is shielded by copper tape. Also, to reduce the common-mode noise, the ferrite beads are combined to measurement cables.

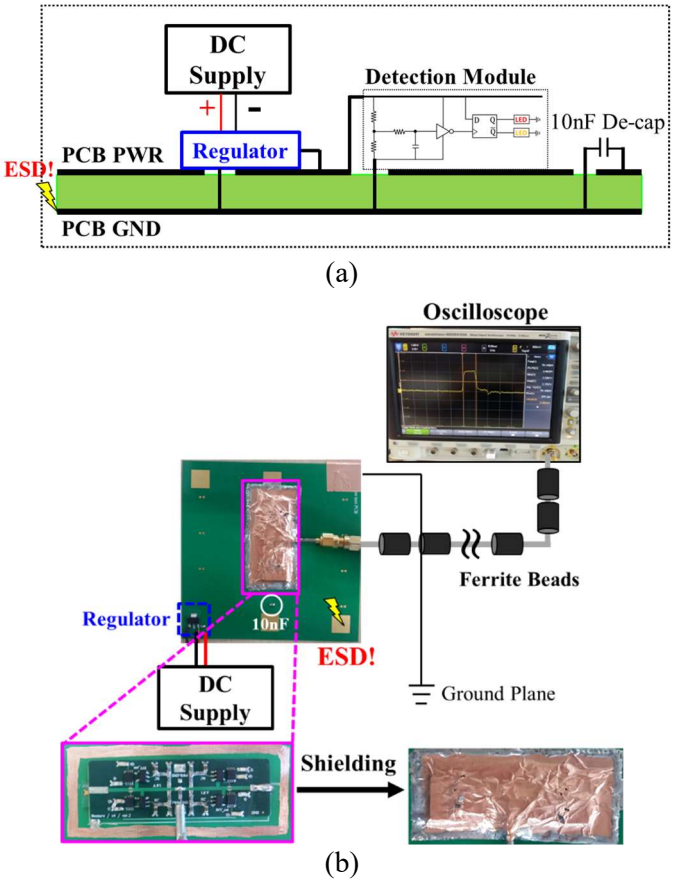
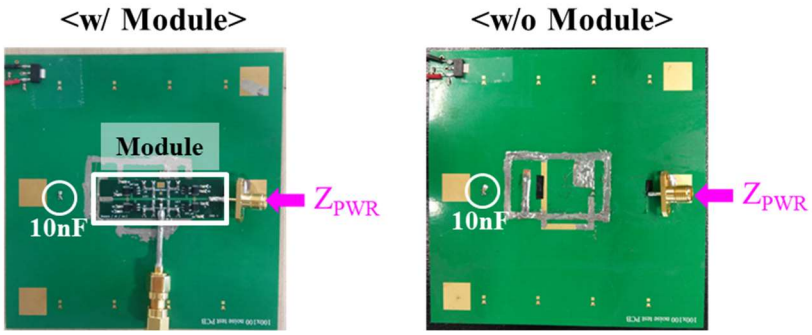
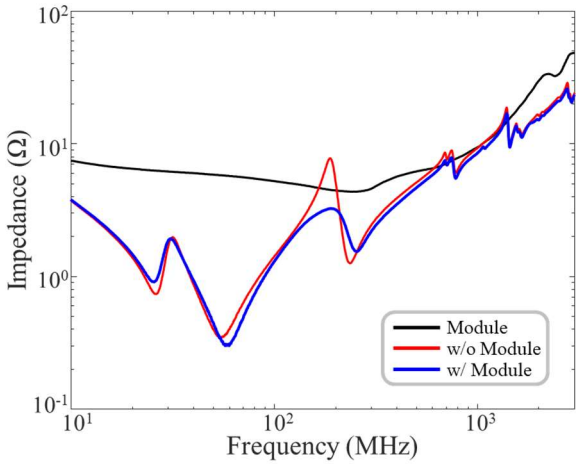


Fig. 17. Test setup for validation of threshold curves using ESD gun (a) Block diagram (b) Simplified drawing with pictures

In the test structure, Z_{PWR} at connection point between PCB PWR of test PCB and VDD net of detection module is measured as shown in Fig. 18 (a). The effects by the parallel installation of module can be investigated by comparing Z_{PWR} plots in test structure according to without module (w/o Module) and with module (w/ Module) cases. In Fig. 18 (b), Z_{PWR} plot of w/o Module case, test PCB itself, has several resonances at frequency range from 10 MHz to 3 GHz, but the difference between impedances at these resonances is mitigated due to a decoupling capacitor of 10 nF on test PCB. Although the module is connected in parallel to PCB PWR of test PCB, Z_{PWR} plots of w/o Module and w/ Module cases agree sufficiently well the except for one anti-resonance where the difference is just about 4 Ω. From these results, it can be found that the parallel connection of detection module to test PCB has negligible effects.



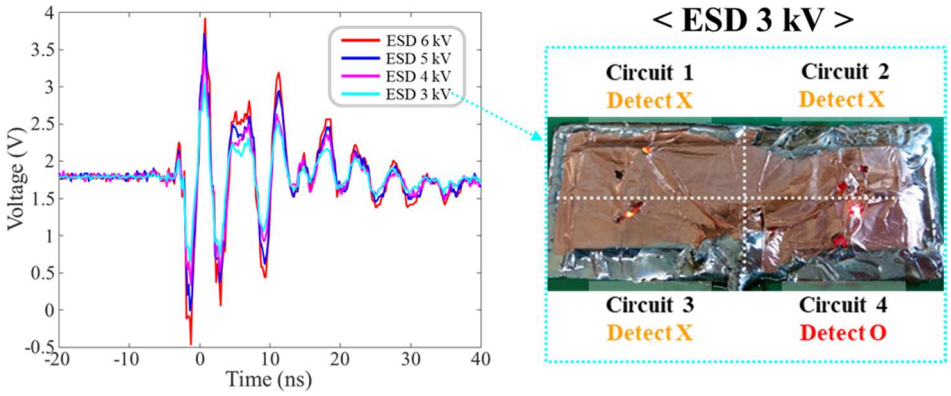
(a)



(b)

Fig. 18. (a) Measurement points for Z_{PWR} in test structure (b) Comparison between Z_{PWR} plots in test structure according to w/o and w/ detection module cases

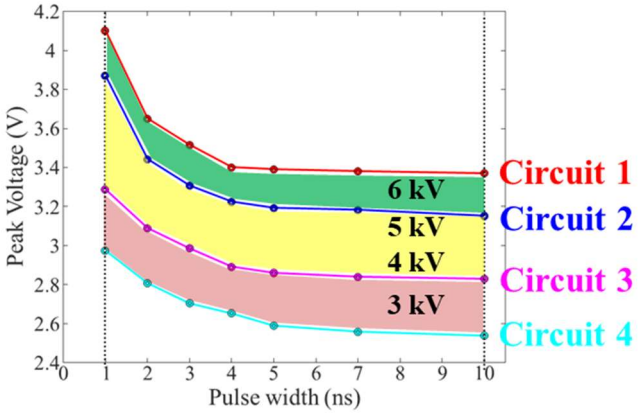
Fig. 19 (a) shows measurement results of ESD noises with various ESD gun levels. The amplitudes are changed but the overall noise shape is almost similar. Fig. 19 (b) is a picture of detection module under ESD gun level of 3 kV where Circuit 4 only senses the ESD event. The ESD current injection tests are repeated 30 times at each ESD gun level and detection of module is summarized as a table as shown in Fig. 19 (c). From this table, the ESD noise range can be estimated like Fig. 19 (d) according to ESD gun level. For example, in case of ESD 3 kV, as Circuit 4 senses the ESD event but Circuit 3 can't detect, the ESD noises at ESD 3 kV has the range above the threshold curve of Circuit 4 but below that of Circuit 3.



(a) (b)

	Circuit 1	Circuit 2	Circuit 3	Circuit 4
6 kV	Detect X	Detect O	Detect O	Detect O
5 kV	Detect X	Detect X	Detect O	Detect O
4 kV	Detect X	Detect X	Detect O	Detect O
3 kV	Detect X	Detect X	Detect X	Detect O

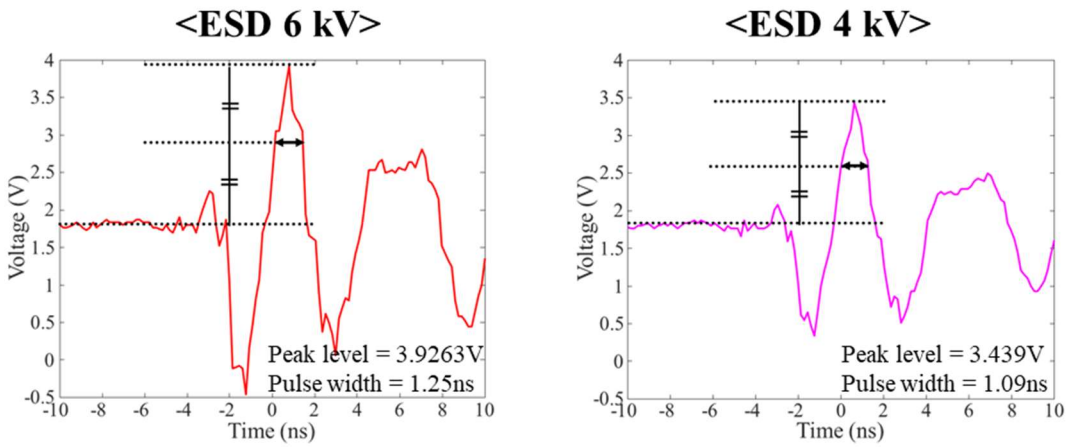
(c)



(d)

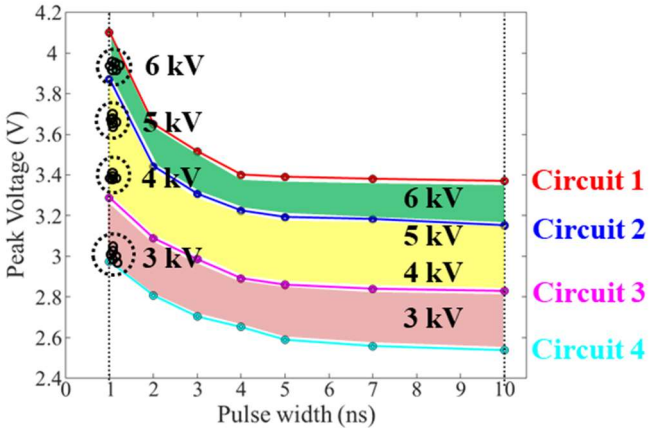
Fig. 19. (a) Measurement results of ESD noises with various ESD gun levels (b) A picture of detection module under ESD gun level of 3 kV (c) Detection of module and (d) the estimated ESD noise range according to ESD gun level

The proposed detection circuit can only sense the positive ESD event. So, the detection occurs from the first positive noise peak of ESD noise. To validate the threshold curves, the peak level and pulse width of the noise peak are checked at each measured ESD noise. Fig. 20 (a) and (b) are zoom-in plots of Fig. 19 (a) at 6 kV and 4 kV ESD levels, respectively. The noise peak data are plotted on the detection threshold curves of Fig. 19 (d). The plotted noise peak data are well grouped and located within the estimated range according to the ESD gun level as shown in Fig. 20 (c).



(a)

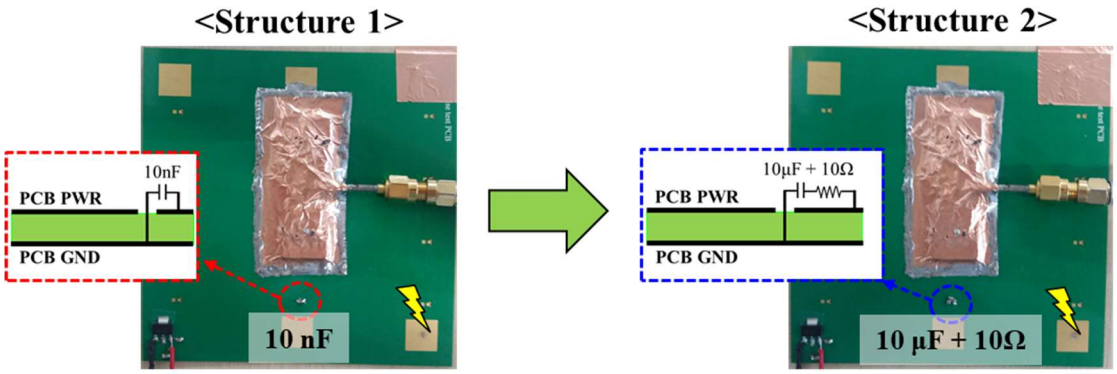
(b)



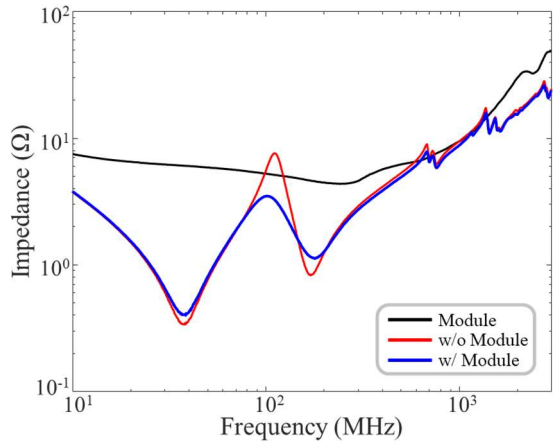
(c)

Fig. 20. The first positive noise peaks of the measured ESD noises at the levels of (a) 6 kV and (b) 4 kV and (c) Comparison between the noise peak data and the estimated ESD noise range according to ESD gun level

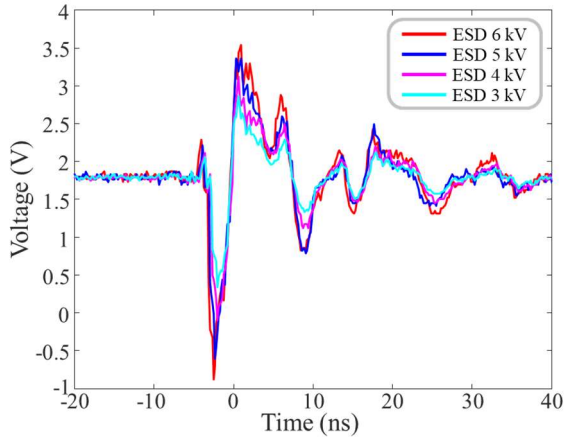
In Fig. 20 (c), the pulse widths of noise peaks are almost same although the ESD gun levels are changed. To validate the threshold curves at other pulse width, the test structure is changed from Structure 1 to Structure 2 by using a decoupling capacitor of 10 μF with series resistor of 10 Ω like Fig. 21 (a). In Fig. 21 (b), similar to Structure 1, Z_{PWR} plots of w/o Module and w/ Module cases in Structure 2 also shows satisfactory agreement except for one anti-resonance where the difference is only about 4 Ω. Compared with Z_{PWR} plots of Fig. 18 (b) in Structure 1, the meaningful discrepancy is observed at less than 300 MHz frequency range, resulting in the significant change of overall noise shape as shown in Fig. 21 (c).



(a)



(b)



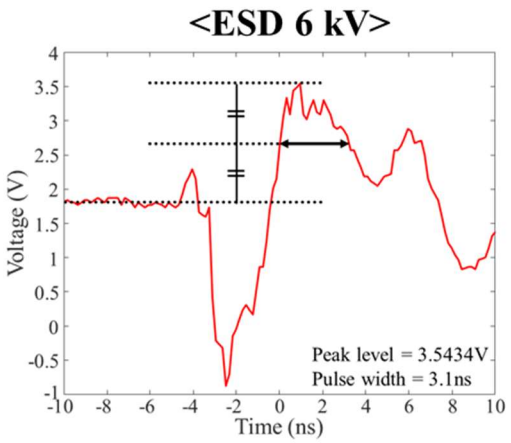
(c)

Fig. 21. (a) Change of test structure by using a different decoupling capacitor with series resistor (b) Comparison between Z_{PWR} plots according to w/o and w/ detection module cases and (c) measurement results of ESD noises with various ESD gun levels in new test structure (Structure 2)

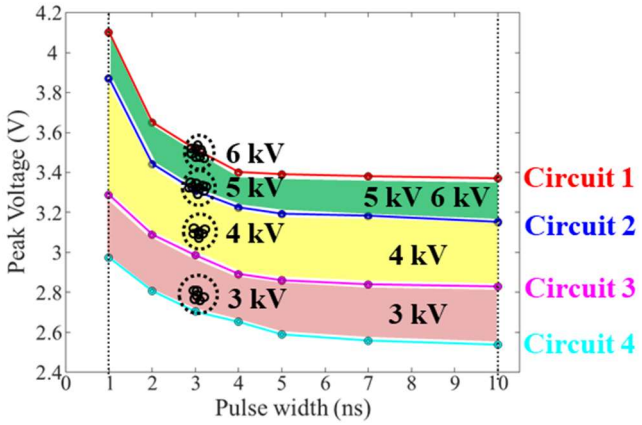
The same validation process is performed again in Structure 2. The ESD current injection tests are repeated 30 times at each ESD gun level and detection of module is summarized as a table as shown in Fig. 22 (a). Also, the peak level and pulse width of the noise peak are checked at each measured ESD noise. Fig. 22 (b) shows the first positive noise peak at ESD 6 kV. Then, the noise peak data are plotted on the detection threshold curves and compared with the estimated ESD noise range from detection of module. Like the previous test structure (Structure 1), the noise peak data are well grouped and located within the estimated range according to the ESD gun level as shown in Fig. 22 (c). As a summary, in two different test structures, the threshold curves of detection module are verified.

	Circuit 1	Circuit 2	Circuit 3	Circuit 4
6 kV	Detect X	Detect O	Detect O	Detect O
5 kV	Detect X	Detect O	Detect O	Detect O
4 kV	Detect X	Detect X	Detect O	Detect O
3 kV	Detect X	Detect X	Detect X	Detect O

(a)



(b)



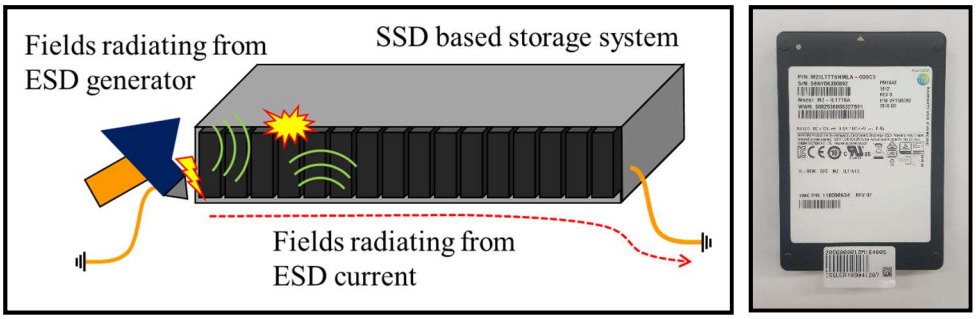
(c)

Fig. 22. (a) Detection of module in Structure 2 according to ESD gun level (b) The first positive noise peak of the measured ESD noise at the level of 6 kV (c) Comparison between the noise peak data and the estimated ESD noise range according to ESD gun level

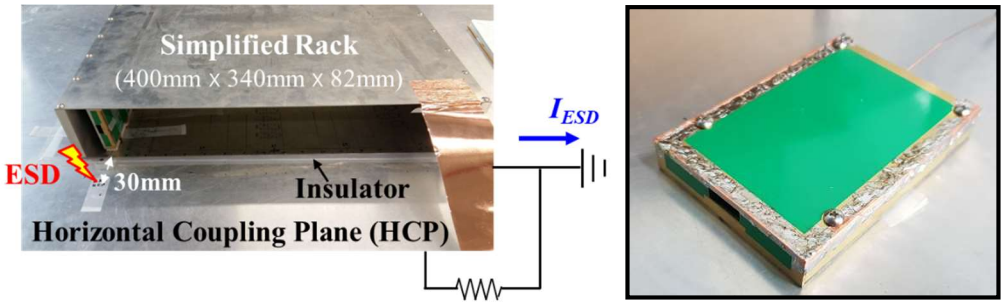
2.3 Application to System-level ESD Analysis in Solid-state Drive (SSD) Storage System

As an application to real situation, the system-level transient ESD noises in a commercial solid-state drive (SSD) storage system in Fig. 23 (a) are characterized and analyzed using the off-chip detection module. In this system, because the electronic product is compact, the connection of cables to measurement point is physically difficult. Fig. 23 (b) represents the simplified situation of Fig. 23 (a) for the easier analysis where a simplified rack is used instead of real data array enclosure (DAE) and only one SSD product is replaced by the simplified chassis with an internal empty PCB. According to the international standard [3], the ESD currents are injected to horizontal coupling plane (HCP) using the ESD gun. The target system to be tested, the rack structure with the simplified SSD product, is separated from HCP through the thin insulating film. The rack structure is shorted to ground plane with

copper tape and the HCP is connected to ground plane with bleed resistors for dissipating the accumulated charges on HCP.



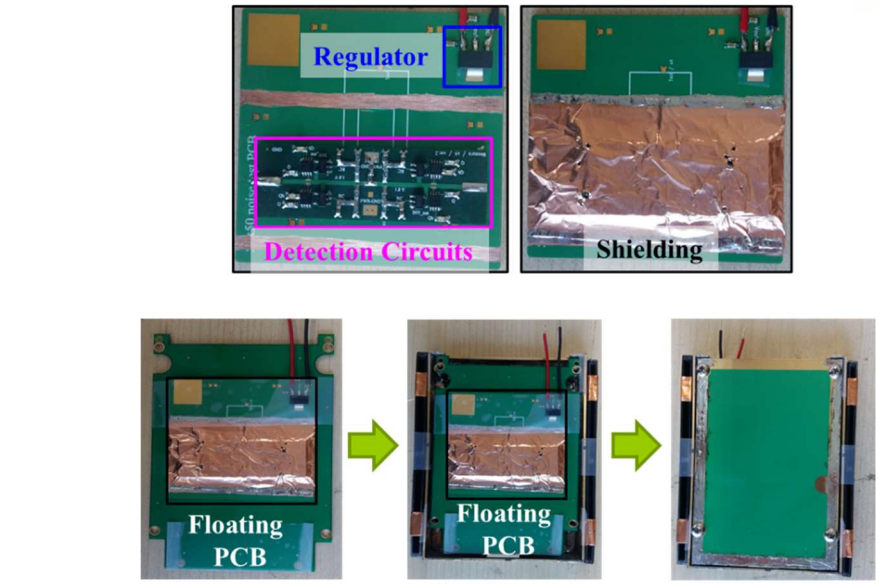
(a)



(b)

Fig. 23. (a) System-level ESD event in a commercial SSD storage system (b) Simplified situation of SSD storage system

For the ESD noise analysis within a in simplified SSD product, the detection module is installed as shown in Fig. 24 (a). The module is connected to power and ground of the dummy PCB where regulator is installed. And, the module is shielded for preventing the directly radiated fields from ESD gun. Then, this dummy PCB with module is attached to internal empty PCB within a simplified SSD chassis using insulating tapes. Fig. 24 (b) and (c) represent the ESD test setup in w/o Rack and w/ Rack cases, respectively. In the simplified system, the ESD currents are injected to HCP in w/o Rack and w/ Rack cases where the injection point is 30 mm away from the bottom side of the rack structure as shown in Fig. 23 (b). In this test setup, the LED colors in detection module can be checked through small slot of simplified chassis as shown in Fig. 25.



(a)

(b) (c)

Fig. 24. (a) Installation of detection module in simplified SSD product and ESD test setup in (b) w/o Rack and (c) w/ Rack cases

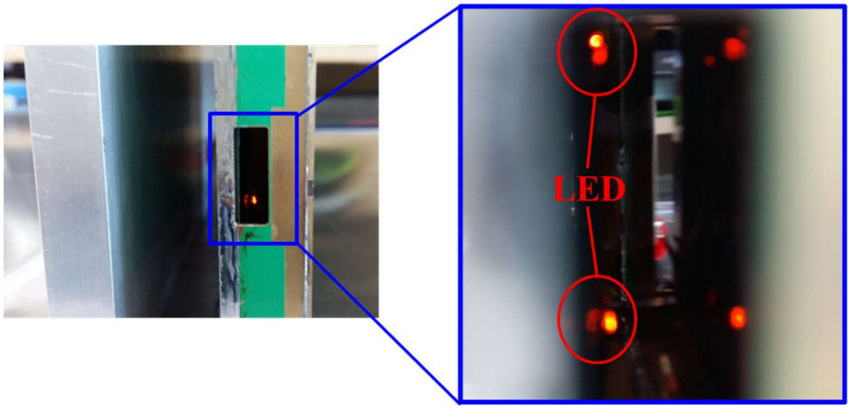


Fig. 25. ESD noise detection by checking the LED colors in detection module through small slot of simplified chassis

Fig. 26 (a) and (b) summarize the detection of module as tables from the turned-on LED colors in w/o Rack and w/ Rack cases, respectively. From these tables, the minimum ESD gun levels for detection

in both cases can be found as shown in Fig. 26 (c) where the threshold ESD gun levels in w/ Rack case are higher than w/o Rack case. Also, the ESD noise range in the simplified system can be estimated in relation to ESD gun level as shown in Fig. 27. For example, in w/o Rack case, the range of the ESD noises by 2 kV level is between the threshold curves of Circuit 2 and Circuit 3 because Circuit 3 detects these noises, but Circuit 2 can't sense. For the deeper analysis, two main noise sources from the ESD generator in Fig. 27 (c) can be considered. The proposed detection module can only characterize ESD noises with less than 1 GHz frequency since the minimum pulse width in the validated threshold curves is limited as 1 ns. So, in w/ Rack case, the ESD noises with below 1 GHz frequency are relatively smaller than w/ Rack case due to the higher threshold ESD gun levels. Also, because the ESD noises with that frequency range mainly are generated by the ESD currents of ESD generator, it can be concluded that the existence of simplified rack structure reduces the ESD noises and improves the immunity against the ESD currents.

<w/o Rack>

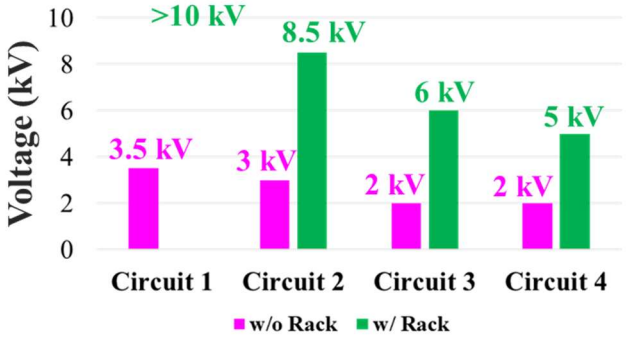
	Circuit 1	Circuit 2	Circuit 3	Circuit 4
3.5 kV	Detect O	Detect O	Detect O	Detect O
3 kV	Detect X	Detect O	Detect O	Detect O
2.5 kV	Detect X	Detect X	Detect O	Detect O
2 kV	Detect X	Detect X	Detect O	Detect O

(a)

<w/ Rack>

	Circuit 1	Circuit 2	Circuit 3	Circuit 4
10 kV	Detect X	Detect O	Detect O	Detect O
8.5 kV	Detect X	Detect O	Detect O	Detect O
6 kV	Detect X	Detect X	Detect O	Detect O
5 kV	Detect X	Detect X	Detect X	Detect O

(b)



(c)

Fig. 26. (a) Detection of module for various ESD gun levels in (a) w/o Rack and (b) w/ Rack cases (c) The minimum ESD gun levels for detection in both cases

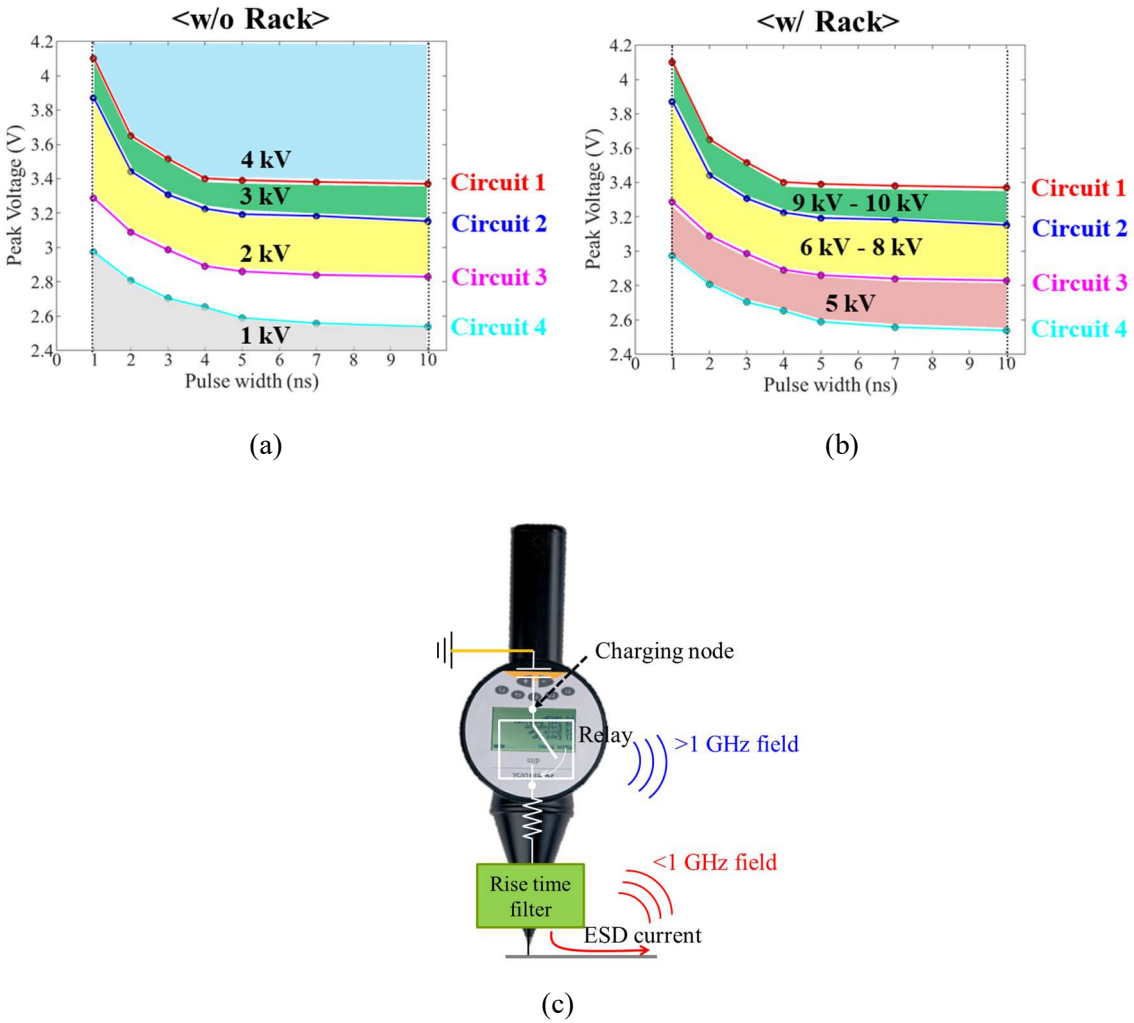


Fig. 27. (a) The estimated ESD noise ranges according to ESD gun level in (a) w/o Rack and (b) w/ Rack cases (c) Two main noise sources from the ESD generator

2.4 Conclusion

In this section, the usage of off-chip ESD detection module including multiple detection circuits with different thresholds is proposed for characterizing the range of ESD noise. At first, the schematic of the proposed off-chip detection circuit and detection process were explained. And, TLP signals were used as controllable noise pulse signals and the threshold curve for the single detection circuit was extracted. Since the detection can be sensed by the color of the turned-on LED, the noise range can be estimated without measurement, utilizing the extracted threshold curve. For better identification of noise range, the detection module including 4 detection circuits with different detection characteristics was designed. The threshold curves of module were extracted using TLP signals again and validated through ESD current injection tests in two test structures. The estimated ESD noise range from detection of module are compared with the noise peak data from measured ESD noises in each case. As a result, the noise peak data are well grouped and located within the estimated range according to the ESD gun level. As

an application to real situation, the detection module was utilized for characterizing and analyzing the system-level ESD noises in a simplified SSD storage system where the measurement of ESD noises is rather difficult and limited physically. Through the detection of module, the threshold ESD gun levels were obtained and the ESD noise ranges were characterized according to the ESD gun level and the existence of rack structure. Considering the noise sources by ESD generator, it was found that the rack structure in a simplified SSD storage system reduces the ESD noises from ESD currents.

III. Design of an On-die Oscilloscope for System-Level Transient ESD Noise Monitoring

3.1 Introduction to an On-die Oscilloscope Circuit

The proposed approach using off-chip detection module can characterize the noise range, but it still has some problems in size and accuracy as shown in Fig. 28. Also, although the on-die circuits from previous researches can provide the useful information such as peak voltage or current level or when a transient stress event ocuurs, it is still further demanded to obtain the accurate noise waveforms for complete analysis. So, as another approach, an on-die oscilloscope circuit for capturing the noise waveform itself like digital oscilloscope is proposed in Fig. 29.

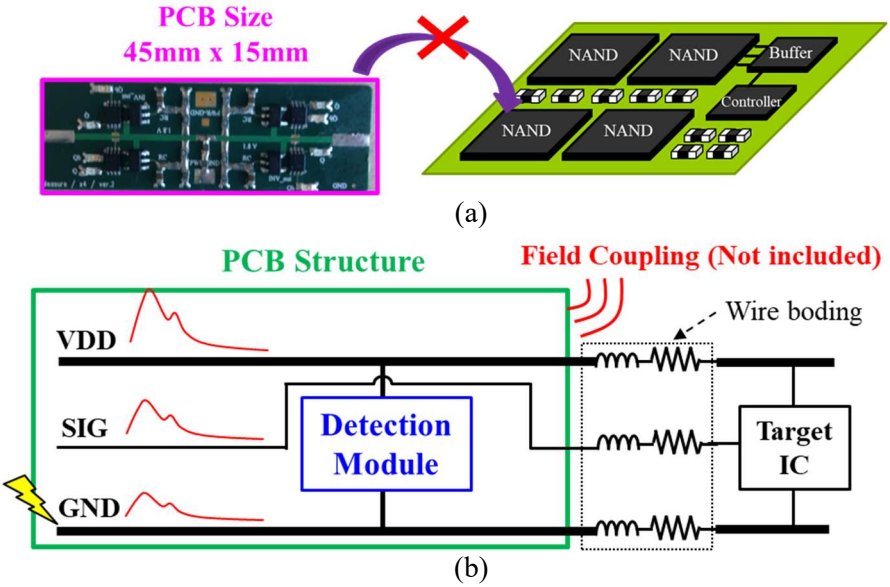


Fig. 28. The problems of a proposed approach using off-chip detection module in (a) space for installation and (b) inaccurate results on PCB-level

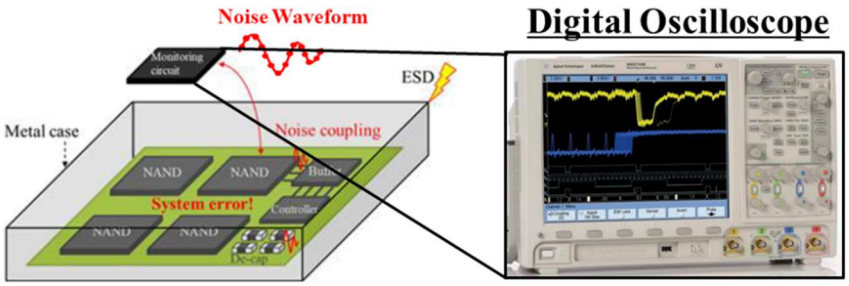


Fig. 29. On-die oscilloscope circuit for capturing the noise waveform itself like digital oscilloscope

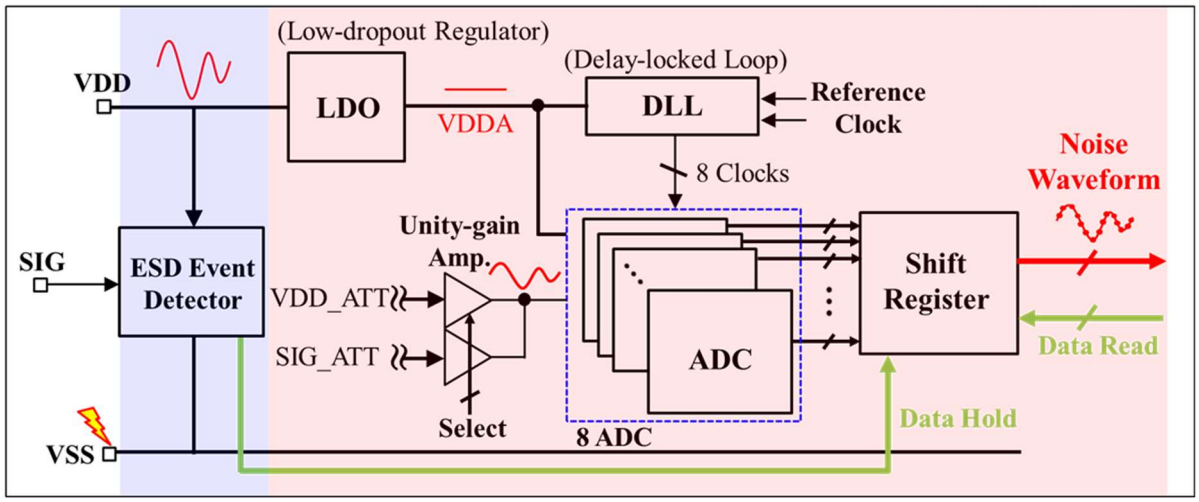


Fig. 30. Block diagram describing the proposed monitoring system

Fig. 30 shows the block diagram describing the proposed monitoring system. This system largely consists of low-dropout regulator (LDO), delay locked loop (DLL), analog-to-digital converters (ADC), shift register, and ESD event detector. Here, there is a "spark" mark at VSS representing the ESD event, but it could be at other external points. Under the ESD event, external power supply and signal lines are contaminated by ESD noise, which can result in malfunction of the system. To prevent the effects by external power supply noise, LDO is utilized for providing the internal power source VDDA, which is robust against the external noise. Among two differential mode voltages, VDD-VSS and SIG-VSS, one waveform is selected and sampled using the multiple ADCs. To sample the noise voltages with large dynamic ranges, the selected waveform is attenuated using resistive voltage division and transferred to ADCs through unity-gain amplifier.

In order to capture the system-level ESD noises with high frequency components over 1GHz, the sampling rate of the system should be sufficiently fast. So, the time-interleaving sampling method is employed in the proposed system. In the proposed monitoring system, 8 ADCs are connected in parallel to enhance the equivalent sampling rate by 8 times of single ADC case. Also, for the sampling clocks used in 8 ADCs, the DLL receives the reference clock and provides eight multi-phase clocks. In each ADC, the noise waveform is sampled, converted to 5-bit binary data, and transferred to the shift register. The shift register is composed of many D flip-flops, storing the binary waveform data from ADCs. When the ESD event detector senses the occurrence of ESD event, a trigger signal (Data Hold) is generated and delivered to the shift register. This trigger signal stops the data shift between DFFs in shift register. If ESD event does not happen, the data delivered by ADCs are shifted continuously and lost at the last DFFs. After the ESD event, the data stored in DFFs are extracted in sequence from the external read command signals (Data Read). The extracted digital data are converted back to analog noise waveform through post-processing.

3.2 Circuit Blocks in the On-die Oscilloscope Circuit

3.2.1 ESD event detector circuits

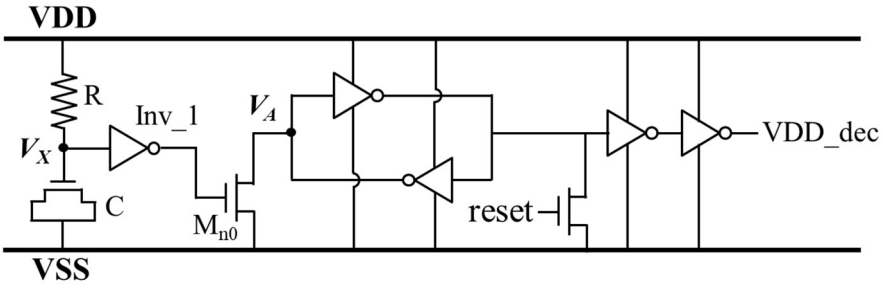


Fig. 31. RC-based ESD detector circuit [14]

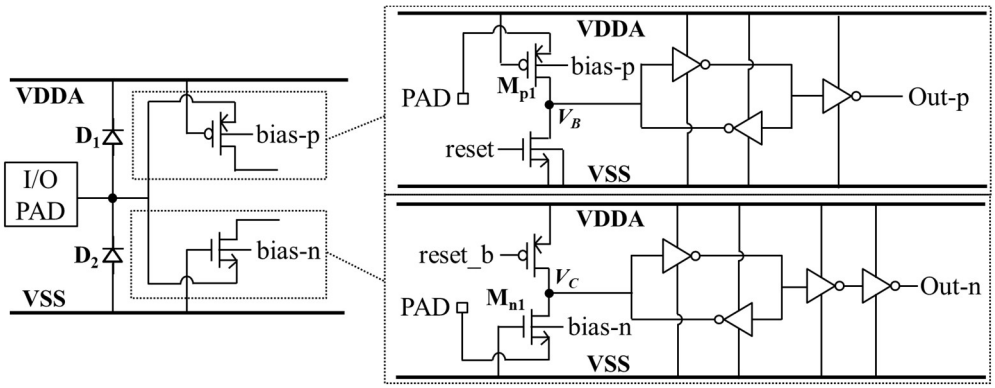


Fig. 32. ESD detector circuit at I/O pad with ESD protection diodes [16]

In the proposed on-die oscilloscope circuit, there are two types of ESD event detector circuits are included. One is located at power supply line and detects the ESD events by power supply noises as shown in Fig. 31. The detection process is as follow. For example, when the VDD level rapidly increases under the positive ESD event, the node V_X shows a slow time response due to a time delay of RC network which has a time constant of few microseconds. So, the level of V_X is relatively recognized as a low state and the output of Inv_1 is changed from low to high state. Then, a NMOS, M_{n0}, is turned-on by the high gate input and the level of V_A becomes low state. Next, the output voltage (VDD_dec) goes to high state from the inverted state of V_A. The output level is maintained due to the latch comprising two inverters until the new reset signal is applied.

The other one is placed near I/O pads and detects the ESD events at I/O pads [16]. As shown in Fig. 32, the detector circuit is mainly consisted of positive and negative event sensors. The detection process is as follow. In the positive event sensor, the level of node V_B is switched to a high state when the voltage across the ESD protection diode D_1 is more than a threshold voltage of M_{p1}. Then, the output voltage (Out-p) is changed to a high state through inverters. The output level is maintained due to the latch like previous detector case. Similarly, in the negative event sensor, the output voltage (Out-n) is

switched from low to high state if the voltage across D_2 is larger than a threshold voltage of M_{n1}. To include both detection cases, two output voltages, Out-p and Out-n, are combined through the OR gate and the resulting output is SIG_dec.

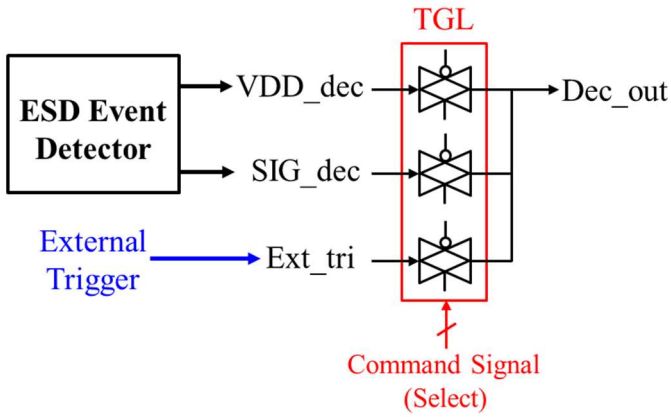
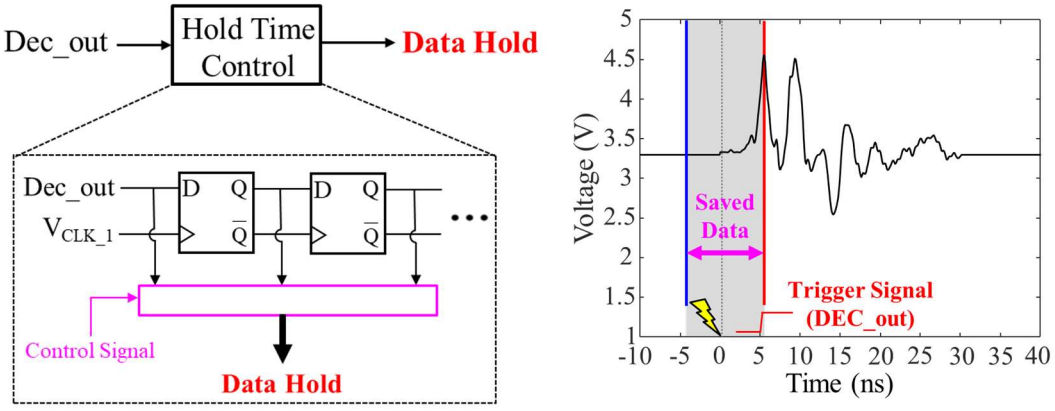


Fig. 33. Logic circuit for selection of ESD event detection modes

As well as two types of detector circuits, an external signal (Ext_tri) generated by an off-chip detector or introduced intentionally is also utilized for detecting ESD events. Two detect signals and one external signal are combined and chosen depending on the intended detection mode, as shown in Fig. 33. A control circuit receives the control signals to select the detection mode and offers command signals, which turn on and off each transmission gate logic (TGL). The selected signal is transferred to a hold time control circuit which adjusts the delay of the trigger signal (Data Hold) as shown in Fig. 34 (a). When the trigger signal is delivered to the shift registers, the waveform digital data during a certain amount of time before the triggering time are saved in the shift registers as shown in Fig. 34 (b). If the trigger signal is immediately delivered to the shift register, the waveform data before that time are extracted but the data after the ESD event cannot be sufficiently available. The hold time control circuit including the serially connected DFFs adjusts the delay of the triggering signal so that the time window for data saving in the shift register is controllable using the command inputs (Time_cont).



(a) (b)

Fig. 34. (a) Hold time control circuit (b) Time window of saved waveform data

3.2.2 Circuits blocks for capturing noise waveforms

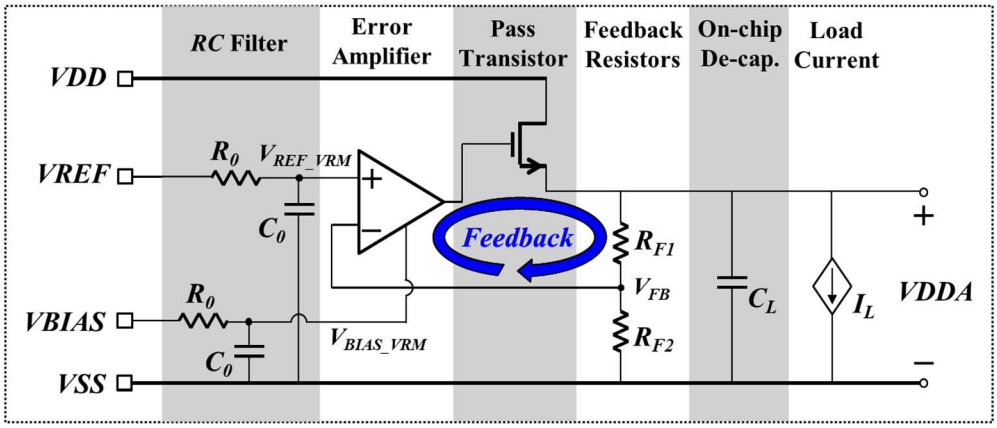


Fig. 35. Schematic of on-chip LDO circuit [19]

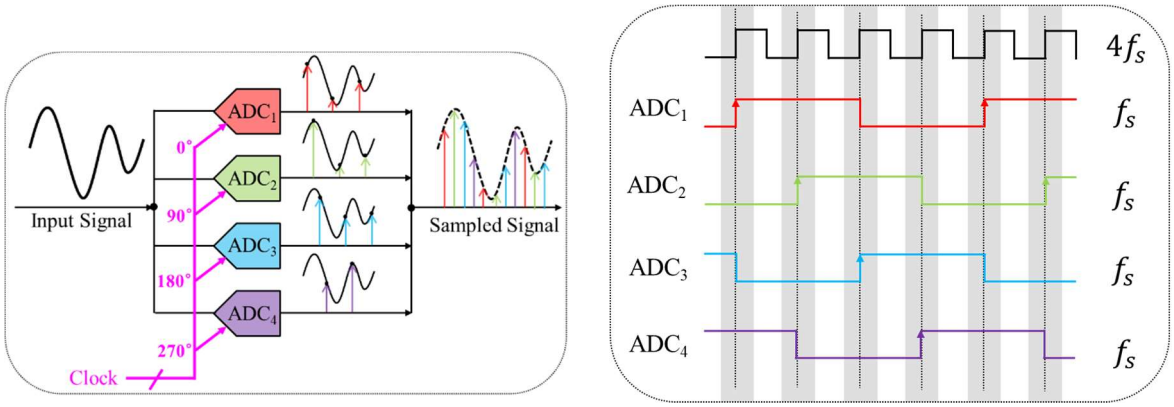
The on-chip LDO circuit is employed to supply internally robust power supply voltage against the ESD noise in the proposed monitoring system. The schematic of a typical on-chip LDO is represented in Fig. 35. The circuit is largely divided into an error amplifier, pass transistor, feedback resistors and on-chip decoupling capacitor at the load [19]. The pass transistor is either turned-on or turned-off according to the levels of the output voltage VDDA and the gate of the pass transistor. So, the voltage level of VDDA converges a specific level through a kind of feedback loop which is decided as

$$VDDA = V_{REF\_VRM} \times (1 + \frac{R_{F1}}{R_{F2}}) \quad (1)$$

In the designed LDO, VDD, VREF and VBIAS are supplied as 3.3V, 1.0V, and 0.8V, respectively. In the designed system, since the target level of VDDA is 1.8V, the values of resistances are 4 kΩ and 5 kΩ at two feedback resistors, R_{F1} and R_{F2}. Because the output voltage VDDA from the LDO acts as a new internal supply voltage at the rest circuit blocks in the proposed whole system, the required load current at LDO is considerable so the size of the pass transistor should be enlarged for having the enough current capacity. Under the ESD events, the external signals of the LDO such as VREF and VBIAS are contaminated by the ESD noises. By inserting the RC filters with R_o = 10 kΩ and C_o = 19 pF, these noises can be filtered out. Also, the ESD noises at VDD are effectively blocked by the RC filter from the turned-on resistance of pass transistor and on-chip decoupling capacitor C_L. For the better noise reduction performance, the larger C_L is desirable due to larger RC time constant at the LDO load; however, it requires a large area and is limited by the chip area, showing the trade-off relationship.

In system-level ESD tests, the frequency components of ESD noises could be over the 1 GHz frequency. The sampling rate of the system should be sufficiently fast to capture the ESD noises. So, in the proposed system, the time-interleaved sampling method is applied. As shown in Fig. 36, by using the multiple and identical ADCs with multi-phase clock signals, the equivalent sampling rate can be increased. In the designed system, the target frequency of single ADC is 800 MHz and 8 ADCs are

combined like this method, resulting in the equivalent 6.4 GHz sampling rate which is enough for sampling of ESD conduction noise waveform.



(a) (b)

Fig. 36. (a) Time-interleaved sampling method (b) Multi-phase sampling clocks

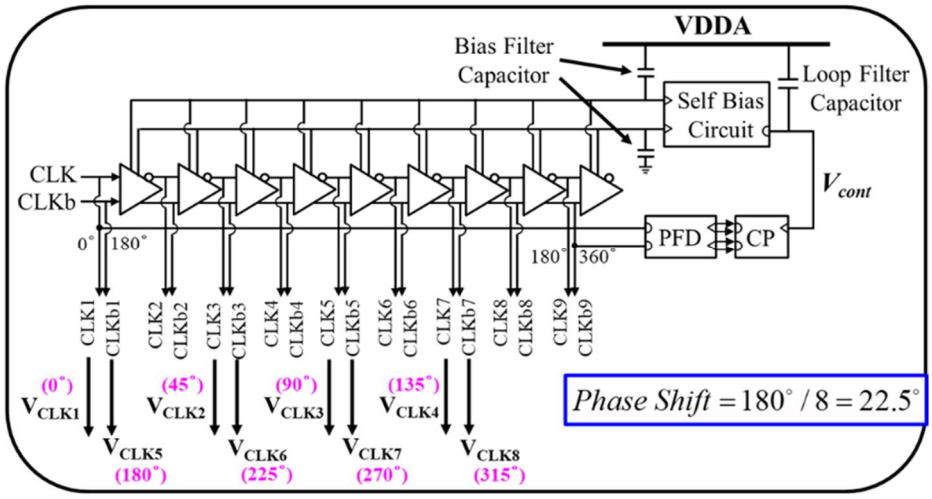


Fig. 37. Simplified block diagram of the designed multi-phase clock generator [20]

Fig. 37 shows the simplified block diagram of the designed multi-phase clock generator using a DLL. The above DLL circuit is largely divided into a delay cell chain, phase frequency detector (PFD), charge pump (CP), and self-bias circuit [20]. In the delay cell chain, 9 delay cells generate the total 18 multi-phase output clocks. Among 18 output clocks in DLL, the marked 8 multi-phase clocks with 22.5° equal spacing are transferred to eight ADCs, as shown in Fig. 37. The locking process is accomplished through the internal feedback loop. In detail, the phases of the reference clock (CLK1) and output clock of the 8-th delay cell (CLKb9) are compared in PDF circuit. For reduction of phase difference, the control voltage V_{cont} from the CP circuit is adjusted. When this control voltage is used as input of the self-bias circuit, the bias voltages of the delay cell chain, V_{bp} and V_{bn}, are also changed for delay control. When the locking process in DLL is completed, the control voltage and two bias voltages become approximately constant level like DC voltage. For the insensitivity against the noise, several filter capacitors are inserted at the control voltage node and bias voltage nodes. Once locking is done, the

phase spacings between the output clocks of DLL are almost kept even under ESD events due to stabilization capacitors.

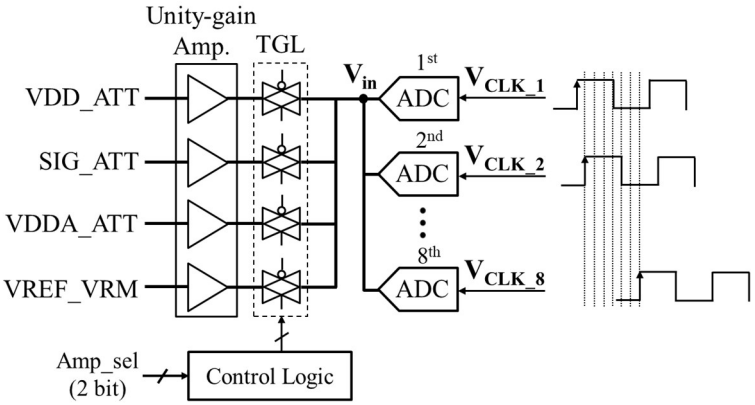
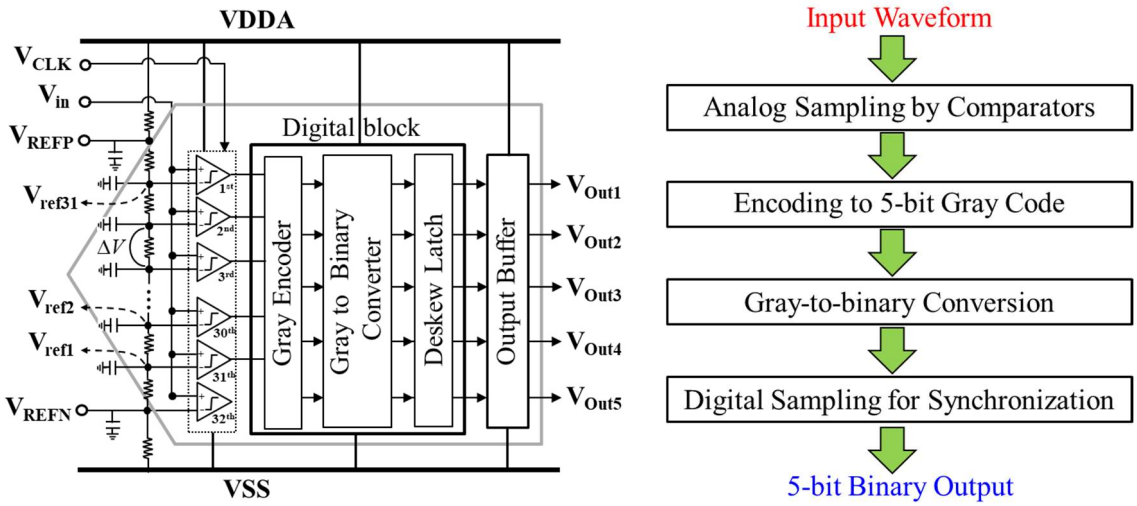


Fig. 38. Selection of the waveform transferred to ADCs for sampling

In the proposed system, one waveform can be selected using the multiple TGLs among four kinds of differential mode voltages, (VDD-VSS), (SIG-VSS), (VDDA-VSS), and (VREF_VRM-VSS) as shown in Fig. 38. Each TGL is turned-on or -off by the amplifier select command inputs (Amp_sel). The selected waveform is delivered to ADCs through unity-gain amplifier.



(a) (b)

Fig. 39. (a) Block diagram of a flash-type ADC [21] (b) Sampling procedure in each ADC

In the proposed on-die oscilloscope circuit, the circuit block playing the most important role is ADC. Fig. 39 (a) depicts the block diagram of the flash-type ADC which demands one cycle for conversion from an analog input to digital outputs. The flash-type ADC includes the reference voltage ladder, comparators, digital block, and output buffer [21]. In the reference voltage ladder, the reference voltages for one input of comparators are derived by the voltage division from the series resistors. In each ADC, there are 32 comparators, and the voltage gap ΔV between the adjacent reference voltages is calculated

as,

$$\Delta V = (V_{REFP} - V_{REFN})/32 \tag{2}$$

In the designed ADC, V_{REFN} and V_{REFP} are set as 0.3V and 1.3V, respectively, and the voltage gap ΔV is about 31.3mV. As shown in Fig. 39 (b), the sampling procedure in each ADC is as follow: First, the comparators receive the selected waveform transferred by the unity-gain amplifier, V_{in}, as one input and the reference voltages from reference voltage ladder as the second input. According to the positive edge timing of the clock signal from the DLL (V_{CLK}), the voltage level of waveform at sampling timing is compared with a reference voltage at each comparator. And, the outputs of 32 comparator are firstly changed to 5-bit gray code in gray encoder. Then, the gray code is converted to binary code and synchronized to the same clock edge through the deskew latch. Because the rates of state change are different in continuous sampling, the inevitable time gap is caused. So, for minimizing the sync error, the digital block including the gray encoder, gray to binary converter, and deskew latch is employed. The gray encoder in the digital block is devised to encode V_{Out1} as the most significant bit (MSB) and V_{Out5} as the least significant bit (LSB). At last, the binary outputs of 5-bit are delivered to the shift register through the output buffer.

The shift register is composed of 128 5-bit DFFs, as shown in Fig. 40. At the same row in register, the 5-bit DFFs share a common clock which comes from an ADC, and the data in previous DFFs are shifted per positive clock edge timing toward the right direction. Since the shift register is devised for saving the waveform data consisted of total 128 sampling points, there are 16 serially connected 5-bit DFFs at each row. Fig. 41 explains the process of sampled digital data according to whether ESD event occurs. If the ESD event does not occur, the data in shift register are shifted continuously and thrown out at the rightmost DFFs in each row. If the trigger signal (Data Hold) is generated and arrived at the shift register, the clock signals in DFFs stick to the low level and the transfer of data between DFFs is stopped. After the ESD event is finished, the stored data in DFFs are extracted in a proper sequence through the external read commands (Data Read) from the first 5-bit DFF to the 128th 5-bit DFF.

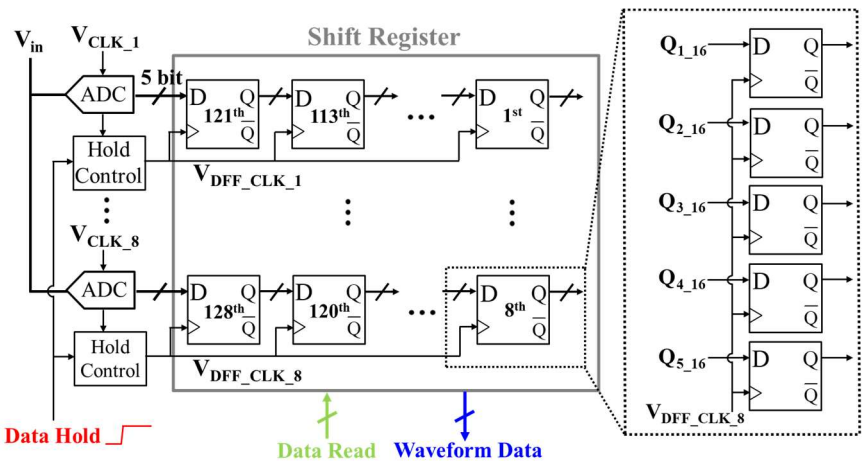


Fig. 40. Shift register composed of 128 5-bit DFFs

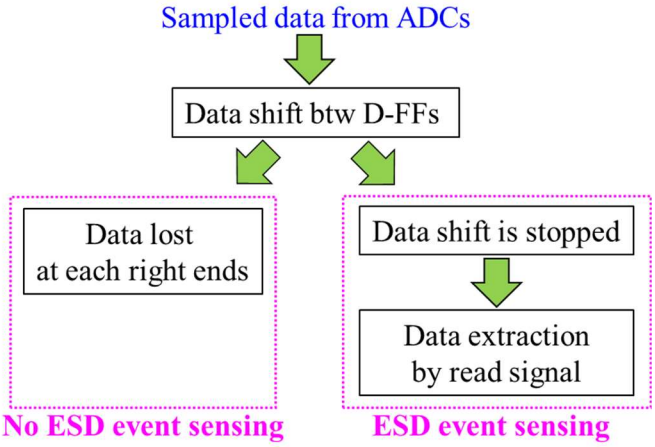
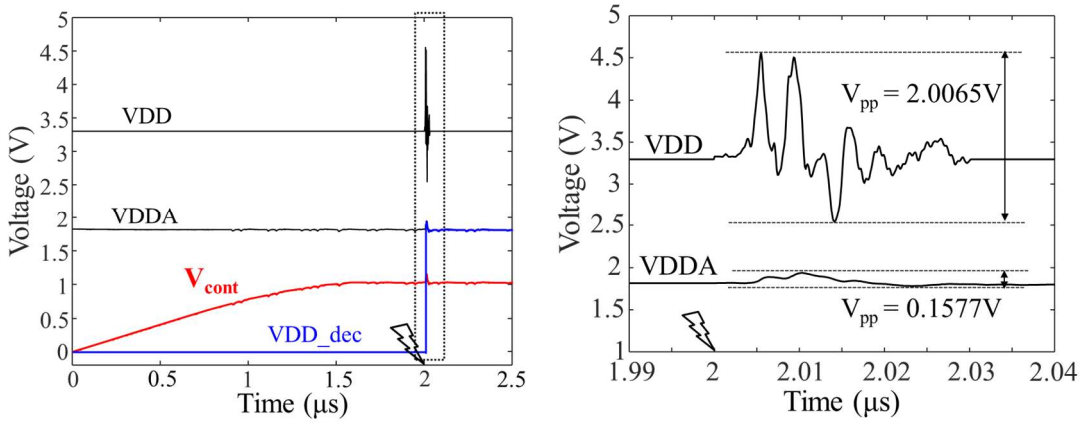


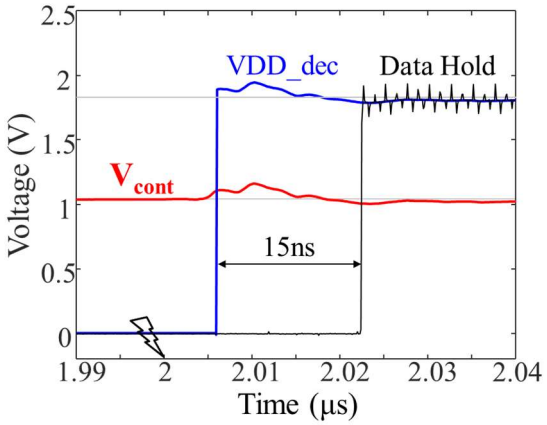
Fig. 41. Process of sampled digital data according to whether ESD event occurs

3.2 HSPICE Simulation of the Designed On-die Oscilloscope

Before fabrication, the operations of circuit blocks in the designed on-die oscilloscope circuit for ESD noise monitoring are tested in HSPICE circuit simulations. As one example imitating the ESD event at power supply line, the measured ESD noise data in Fig. 7 are used for the circuit simulation. To sample and monitor the power supply noise voltage, the attenuated voltage at VDD-VSS is selected in Fig. 38 and the trigger signal generated from the detector circuit at power supply line is chosen in Fig. 33. A 800 MHz is used for the reference clock of DLL in the simulation, which results in a sampling time of 156 ps (64 sampling points in 10 ns).



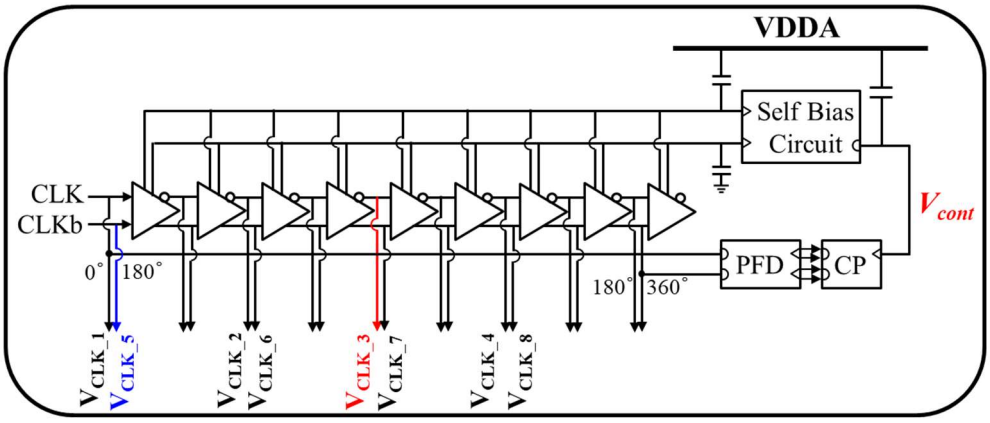
(a) (b)



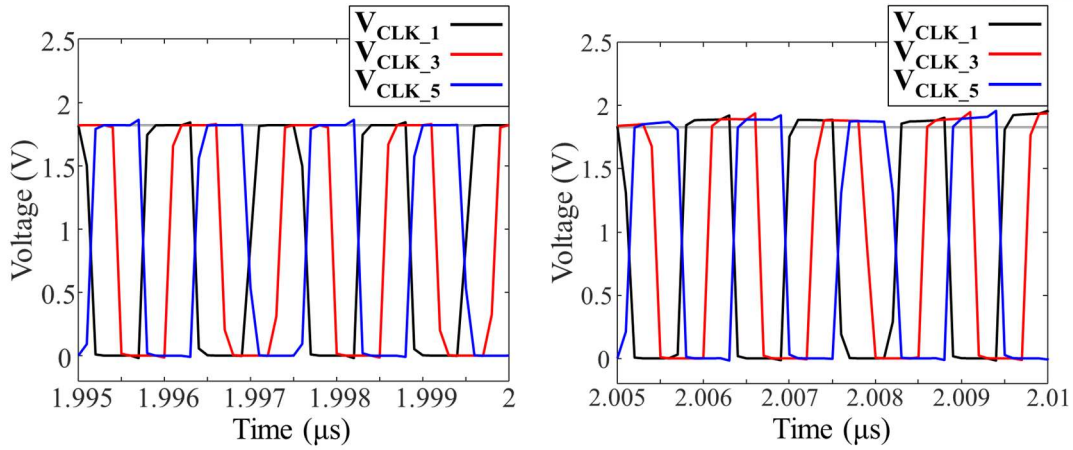
(c)

Fig. 42. Results of circuit simulations (a) Injected ESD noise data at 2 μs (b) Comparison the voltage fluctuations at VDD and VDDA (c) ESD event detection

The transient circuit simulation results of the proposed on-die oscilloscope are shown in Fig. 42. The locking process in DLL is finished later than 1.5 μs, as shown in Fig. 42 (a). So, the measured ESD noise data at power supply line is injected into VDD-VSS at 2 μs. The voltage fluctuation at the VDD by the ESD noise is effectively filtered out by the LDO, as shown in Fig. 42 (b). The levels of peak-to-peak voltages are 2.0065V at VDD but 0.1577V at VDDA. When the timing of voltage waveforms at VDD and VDD_dec are compared, it is found that the detector circuit at power supply line can detect the ESD event occurrence from the first noise peak at the VDD. The generated trigger signal from the detector circuit for holding the saved waveform data in the DFFs is delayed by 15 ns from the VDD_dec signal, as shown in Fig. 42 (c).



(a)



(b) (c)

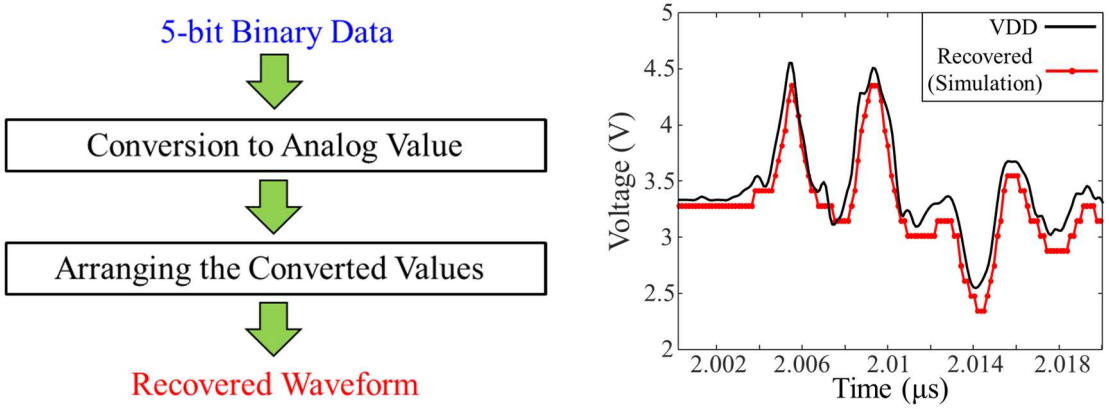
Fig. 43. (a) The block diagram of multi-phase clock generator (b) Magnified plot for 5 ns before the ESD noise injection (c) Magnified plot for 5 ns after ESD noise injection

Fig. 43 represents the block diagram of multi-phase clock generator and the three output clocks of the DLL in the circuit simulation under the ESD event. When the shapes and levels of clock signals are compared before and after the ESD noise data injection in Fig. 43 (b) and (c), the levels are slightly deviated with respect to the level in the normal operation condition due to the small variation of VDDA, but the phase difference between the clocks is almost maintained, implying robustness to the ESD noise.

The sampled waveform data in the shift register are extracted applying the external read command signals after the ESD noise is completely gone and the power supply voltage becomes steady-state level. The extracted waveform data are recovered to an analog waveform by post-processing as explained in Fig. 44 (a). The obtained 5-bit binary data from extraction process can be translated to a decimal number DAC and analog value DAC_A as, respectively,

$$DAC = (Q_1 \times 16 + Q_2 \times 8 + Q_3 \times 4 + Q_4 \times 2 + Q_5 \times 1)/1.8V \quad (3)$$

$$DAC\_A = V_{REFN} + \Delta V \times DAC \quad (4)$$



(a) (b)

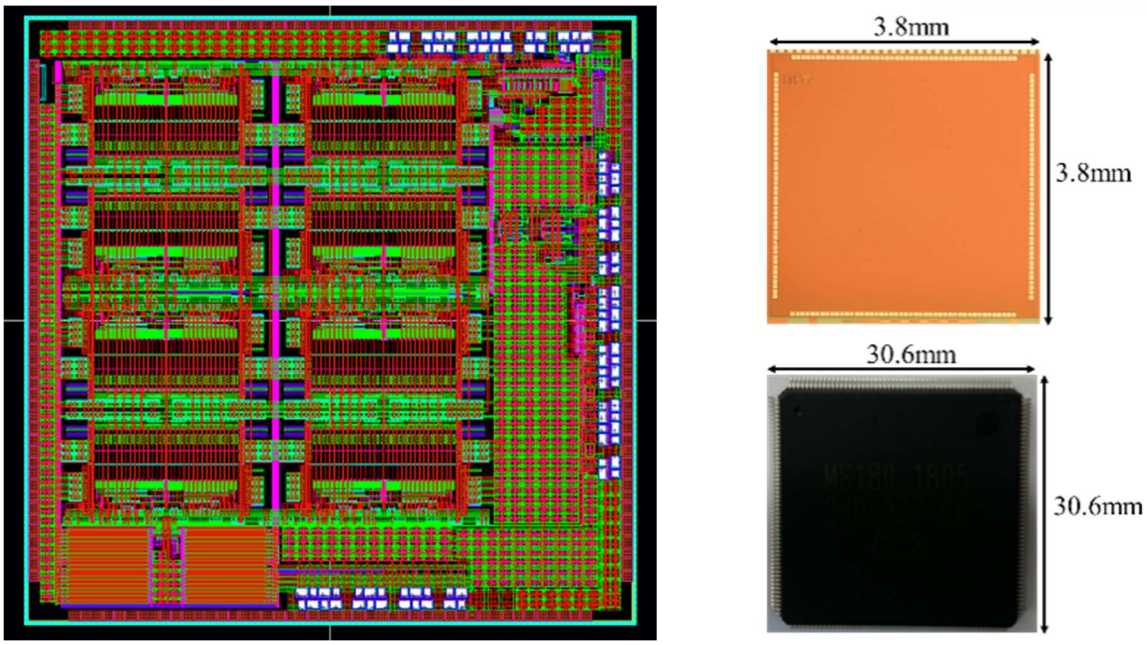
Fig. 44. (a) Post-processing for recovering waveform (b) Comparison between the applied noise voltage at VDD and the recovered analog waveform from the designed circuit

The DAC_A values from (3) and (4) are aligned along with the corresponding time sequence with the time step of 156 ps. Because the actual voltage waveform to be sampled is attenuated before passing through the unity-gain amplifier, as shown in Fig. 38, the attenuation ratio by resistive voltage division should be considered. So, the attenuation ratio is multiplied inversely to the DAC_A values. In the designed circuit, the attenuation ratio from VDD to VDD_ATT was (3.3:0.8).

Fig. 44 (b) shows the comparison between applied noise voltage at VDD and the recovered analog waveform. In the rapidly fluctuating regions at VDD, there are some differences between two waveforms. But the overall shapes agree sufficiently well. Because of the limitation of sampling time in the ADC and the frequency characteristics of the unity-gain amplifier, the discrepancies happen at the high frequency noise components. As a summary, it is found that the designed on-die oscilloscope circuit can display the system-level ESD noise which is seen inside the IC like digital oscilloscope.

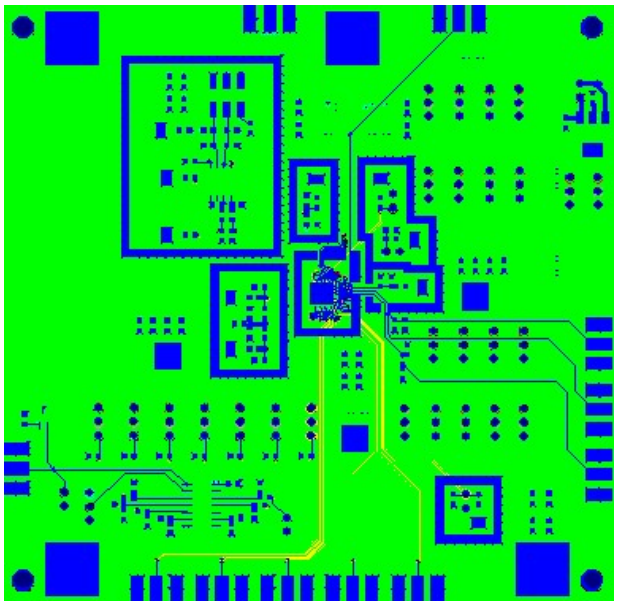
3.4 Validation of Chip Operations in Measurement

The designed circuit is implemented in 180 nm CMOS technology for testing in measurement. Fig. 45 shows the layout of the designed circuit and fabricated die chip and packaged IC as metric quad flat pack (MQFP) type. The sizes of die chip and package are 3.8mm × 3.8mm and 30.6 mm × 30.6 mm, respectively. There are 208 pins in package and only 66 pins are needed for the operation. Also, over 20 pins are used for controlling the operation of chip. The layout of a designed test PCB for validation of the chip operations is shown in Fig. 46 (a) where the size of a test PCB is 112 mm × 110 mm. Fig. 46 (b) shows the test PCB and a picture of a die chip bonded to the PCB. In case of package, the longer wire bonding makes the parasitic inductances between PCB pads and pins of chip which would cause the distortion at high frequency and inaccurate measurement results.

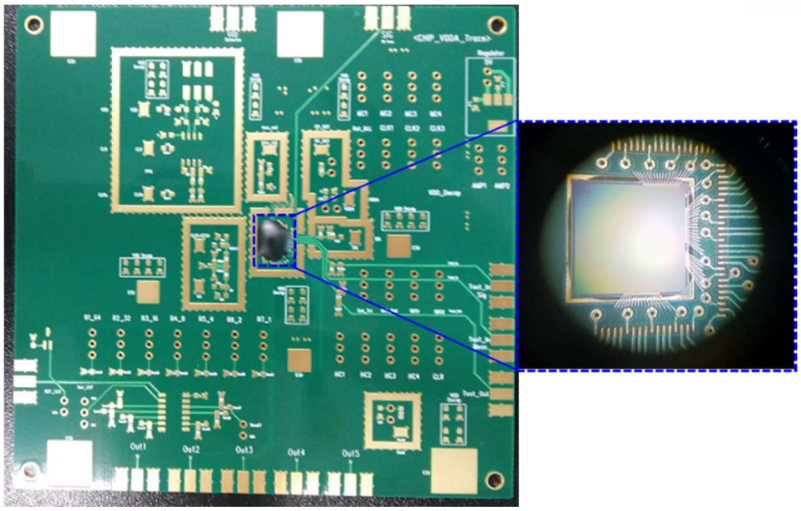


(a) (b)

Fig. 45. (a) Layout of the designed circuit in 180nm technology (b) Die chip and packaged IC with size



(a)



(b)

Fig. 46. (a) Layout of a test PCB for validation of the chip operations (b) Test PCB and a die chip bonded to the PCB

Fig. 47 shows the measurement setup for testing the operation of capturing the noise waveform in the designed circuit. Testing of the designed circuit is performed in three steps. First, the operation of DLL circuit block will be checked from the low frequency to high frequency. The clock signal for reference clock of DLL is applied to the chip from a pulse pattern generator (PPG). The expected highest locking frequency from the simulation was up to 800 MHz. But, due to several problems in circuit design process, the maximum possible clock frequency is about 300 MHz in measurement. Then, sinusoidal signals with various frequencies are applied into signal line of the chip from the signal generator. Because of low frequency of sampling clocks, the available frequency in sinusoidal signals is limited below 600 MHz. Fig. 48 shows the comparison between the applied signals from signal generator and the recovered waveforms from the on-die oscilloscope circuit at 50 MHz and 100 MHz sinusoidal signals. The offset levels of recovered waveforms are adjusted. As shown in Fig. 48 (b), the ability of waveform capturing is under the designed specification. In detail, -3dB frequency in waveform recover was about 63 MHz.

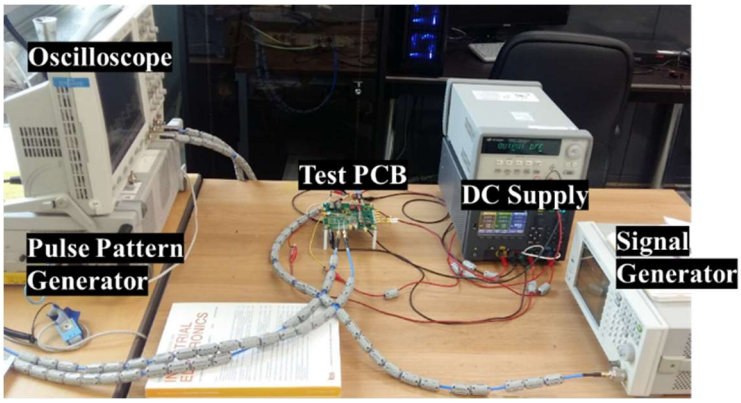
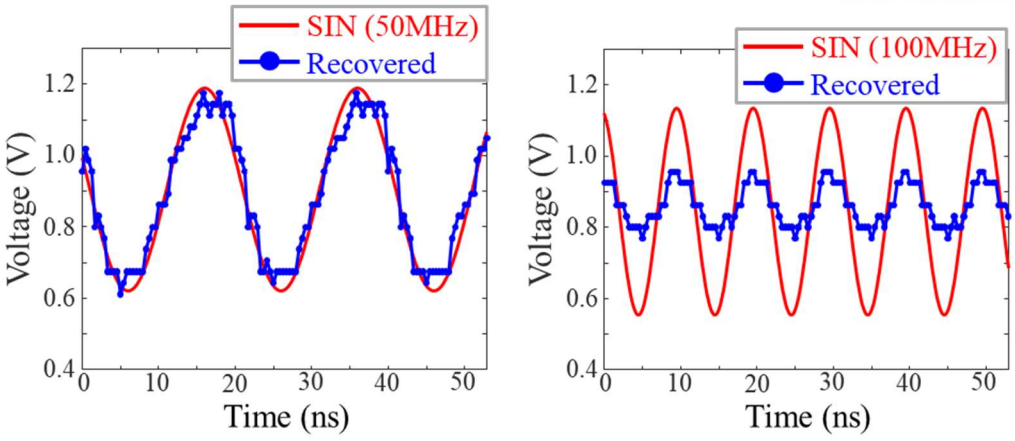


Fig. 47. Measurement setup for validation of operations of the designed circuit



(a) (b)

Fig. 48. The comparison between the applied sinusoidal signals and the recovered waveforms from the on-die oscilloscope circuit (a) at 50 MHz and (b) 100 MHz

Fig. 49 shows the test setup for ESD detector circuit at power supply line. As a noise source, TLP signals described in section II are utilized for finding the detection range. Fig. 50 shows the measured voltages at VDD and detect signals when the pulse width is set as 5.4 ns in TLP generator. Due to low impedance at VDD-GND, the large portion of the noise signal is reflected, and then, the reflected signal is injected again into ESD detector circuit at power supply line. By multiple reflections, the measured voltages at VDD show the ringing shape with several noise pulses. As shown in Fig. 50 (b), if the voltage level of the first noise pulse is over the threshold, the detect signal is switched from low to high level. Fig. 51 represents comparison of detection threshold curves between circuit simulation and measurement. The procedure of extraction of threshold curve is equal to that in section II. In simulation, the threshold curve is flat up to pulse width of 2 ns. The threshold level increased sharply in the shorter pulse width. The threshold curve in measurement also shows the almost flat shape up to pulse width of 5.4 ns. But, due to problems in circuit design process, the results below 5 ns cannot be obtained.

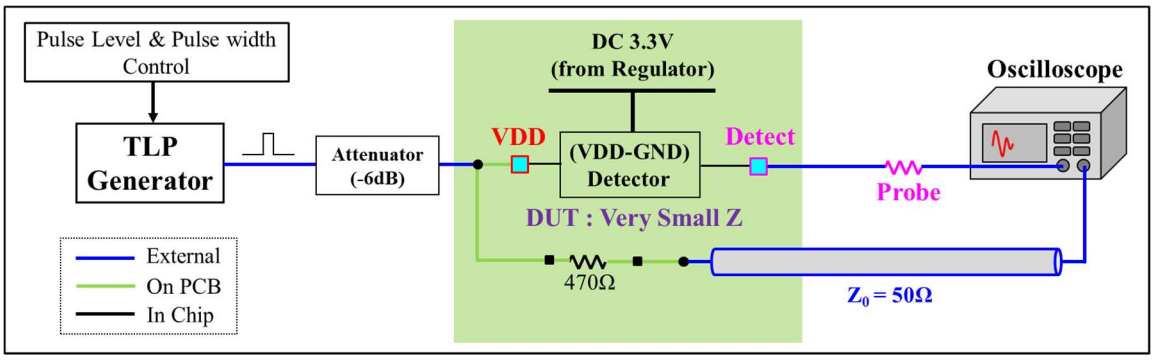
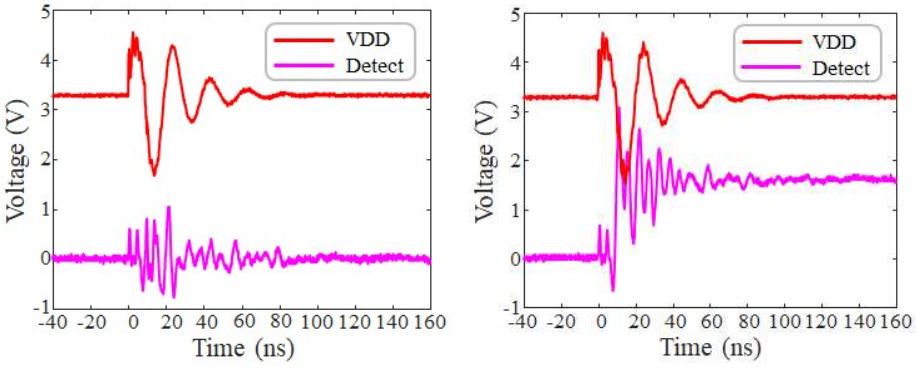


Fig. 49. Test setup for ESD detector circuit at power supply line



(a) (b)

Fig. 50. The measured voltages at VDD and detect signals when the pulse width is set as 5.4 ns in (a) No detect case and (b) Detect case

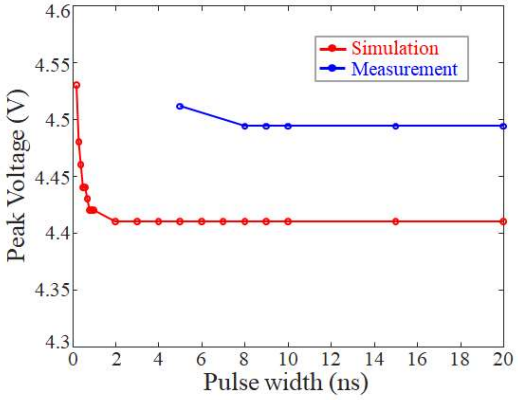


Fig. 51. Comparison of detection threshold curves between simulation and measurement

Fig. 52 shows the test setup for ESD detector circuit at signal line. As in case of ESD detector circuit at power supply line, TLP signals are utilized for finding the detection range. But, due to the soldered resistor on test PCB, the impedance at SIG-GND is almost 50 Ω and the reflection issue does not need to consider. Fig. 53 and Fig. 54 represent the measured voltages at SIG and detect signals from positive and negative sensors when the pulse width is set as 5 ns, respectively. The comparisons of threshold curves from simulation and measurement in positive and negative sensors are shown in Fig. 55. The procedure of extraction of threshold curves is same as previous ESD detector case. The minimum pulse width in measurement is about 0.6 ns because of limitation in TLP generator. In the common pulse width range, the shapes of threshold curves are nearly flat. There are just small discrepancies in simulation and measurement, which is caused by difference in test environment.

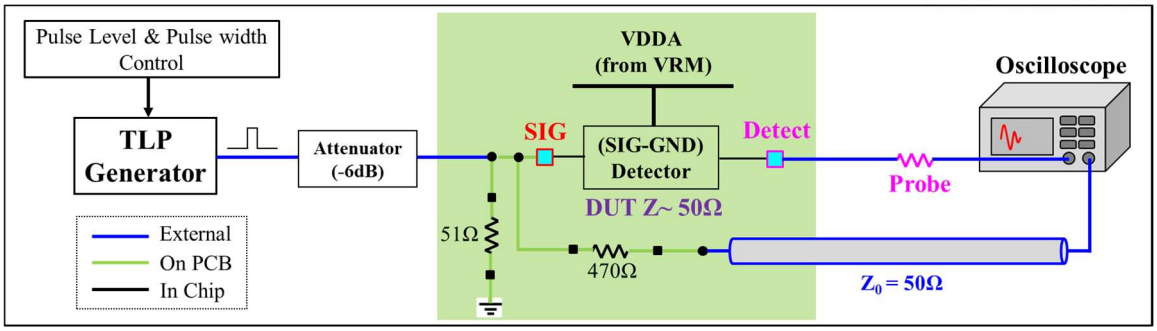
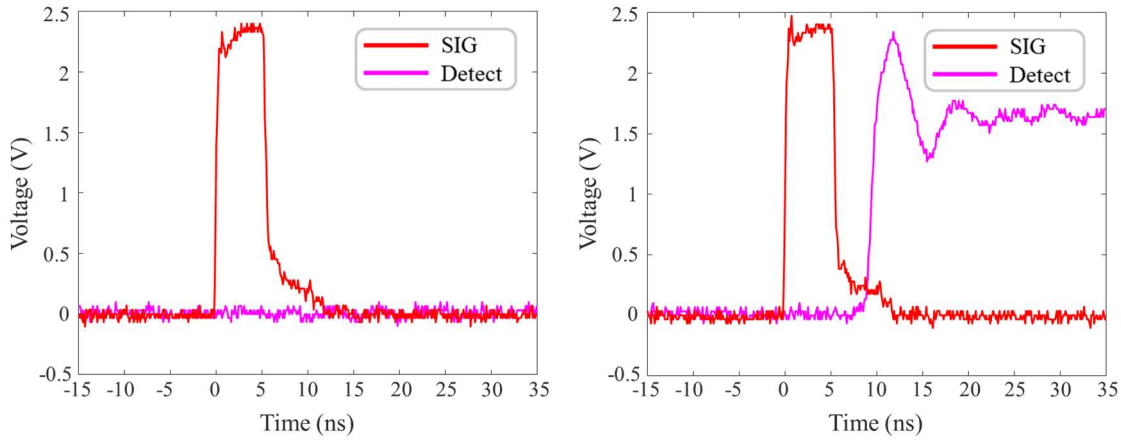
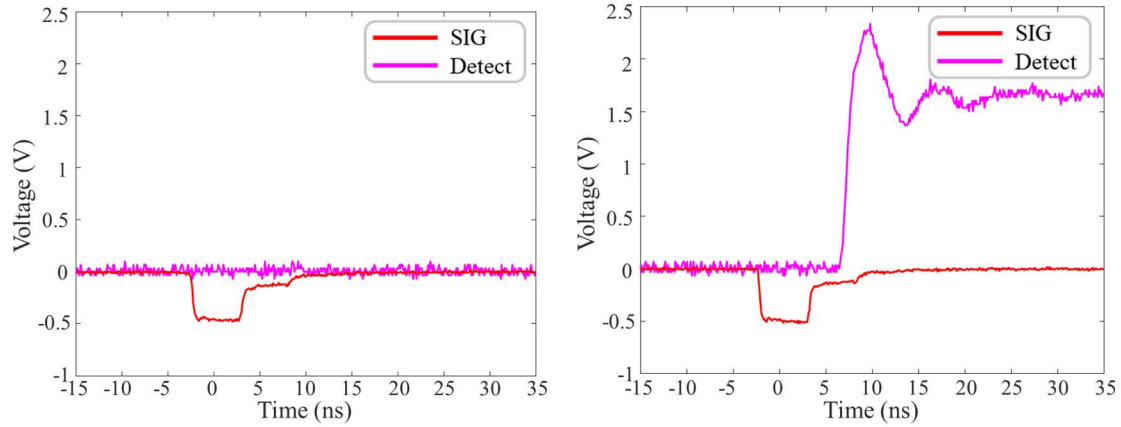


Fig. 52. Test setup for ESD detector circuit at signal line



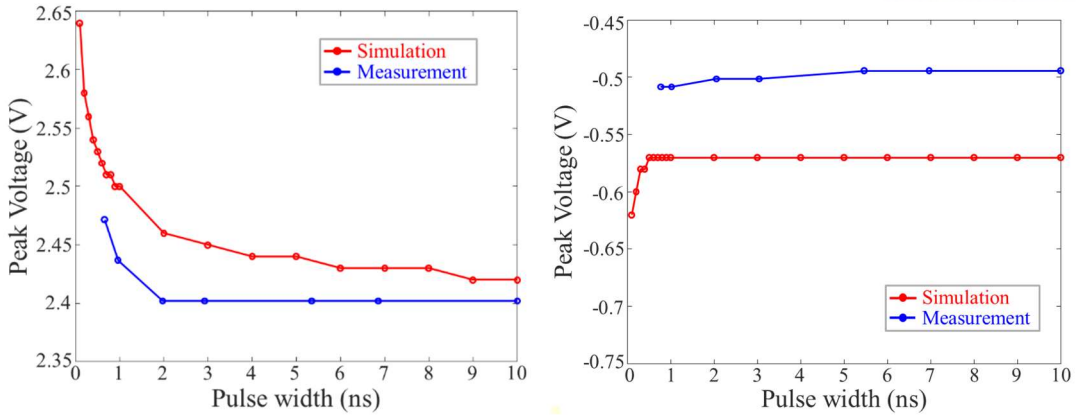
(a) (b)

Fig. 53. The measured voltages at SIG and detect signals from positive sensor when the pulse width is set as 5 ns in (a) No detect case and (b) Detect case



(a) (b)

Fig. 54. The measured voltage at SIG and detect signal from negative sensor when the pulse width is set as 5 ns in (a) No detect case and (b) Detect case



(a) (b)

Fig. 55. Comparisons of threshold curves from simulation and measurement in (a) positive sensor and (b) negative sensor

3.5 Conclusion

In this section, an on-die oscilloscope circuit for monitoring system-level transient ESD noises is proposed as another approach to capture the noise waveform itself like digital oscilloscope. In order to sense the occurrence of ESD events, there are two kinds of on-die detector circuits in the designed circuit. The typical on-chip LDO circuit with RC filters and internal feedback loop is utilized to supply a internally robust power voltage against the ESD noises under ESD event occurrences. In order to capture the system-level ESD noises with high frequency components over 1 GHz, the time-interleaving sampling method is employed in the proposed monitoring system. Parallel connected 8 ADCs enhance the equivalent sampling rate by 8 times of single ADC case. Also, for the sampling clocks used in eight ADCs, the multi-phase clock generator using a DLL is used and provides eight multi-phase clocks. The ESD noise waveforms at power supply or signal line are sampled in ADCs and these sampled data are stored in the shift register. After the ESD event is finished, the stored waveform data in the shift register are extracted in sequence from the external read commands. The extracted digital data are translated and converted back to analog noise waveform through post-processing. The operations of the circuit blocks in the designed circuit are tested in circuit simulations, applying the measured ESD noise data on PCB-level to the power supply line of the proposed system. The noise waveform is sampled, extracted, and recovered to analog waveforms. The recovered waveform from the designed circuit represents enough agreements with the injected ESD noise waveform within the maximum 15% error. The proposed on-die oscilloscope circuit including on-chip ESD detectors is designed and fabricated in 180 nm CMOS process. The validation of operation is performed, and the measurement results of on-chip ESD detector at signal line are comparable to the results from circuit simulations. However, on-chip ESD detector at power supply line and the ability of waveform capturing are under the designed specification due to several problems in circuit design process.

IV. Conclusion and Summary

In this thesis, two approaches to monitor the system-level transient ESD noises were proposed. One is the usage of off-chip ESD detection module including multiple detection circuits with different thresholds is proposed for characterizing the range of ESD noise. As another approach, capturing the noise waveform itself like digital oscilloscope is proposed, designing the monitoring circuit for system-level transient ESD noises.

First, the off-chip detection circuit using time-delay of RC network was proposed. Transmission line pulse (TLP) generator is used as noise pulse generator due to controllable amplitude and pulse width of pulse signal. According to extraction procedure, the threshold curve for the single detection circuit can be extracted. For better identification of noise range, the detection module including 4 detection circuits with different detection characteristics was designed. The threshold curves of module were extracted using TLP signals again. For validation of extracted threshold curves, the ESD currents were injected through ESD generator. Depending on the level of ESD generator, the measured results were plotted on threshold curves and the results were well matched to the estimated ESD noise range from the detection of module. Therefore, the extracted threshold curves are validated. As an application to real situation, the system-level ESD noises in a commercial SSD storage system were characterized and analyzed. In this system, because the electronic product is compact, the connection of cables to measurement point is physically difficult. By analyzing the threshold ESD gun levels of detection module, the ESD noise range can be estimated according to the ESD gun level. Also, associating with the noise sources by ESD generator, it can be found that the rack structure in a simplified SSD storage system reduces the ESD noises from ESD currents.

Second, an on-die oscilloscope circuit for capturing the transient ESD noise waveform is designed. In the designed circuit, the ESD noise waveforms at power supply line or signal line are monitored by sampling and converting to digital data via multiple ADCs. Also, the on-chip ESD event detector circuits detect the ESD event occurrence, characterize the ESD noise range, and generate a trigger signal for keeping the sampled waveform data. The digital data in the shift register are extracted and recovered to noise waveforms through post-processing process. The proposed circuit is designed with 180 nm CMOS technology library. The operations of the circuit blocks in the designed circuit are checked in HSPICE circuit simulations. The input noise waveforms are compared with the recovered waveforms. The designed circuit is fabricated in a 180 nm CMOS process and the validation of operation is performed in measurement. The measurement results of on-chip ESD detectors are comparable to the results from circuit simulations. However, the ability of waveform capturing is under the designed specification due to several problems in circuit design process.

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